

## LPC-P2919 development board

## Users Manual



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## **INTRODUCTION:**

**LPC-P2919** board is easy to use development board with LPC2919 - ARM9 microcontroller with CAN and LIN produced by NXP Semiconductors.

With LPC-P2919 you can explore the features of LPC29XX family on budget, the board has everything necessary to build simple applications: reset and oscillator circuits, JTAG port for programming and debugging, CAN, LIN, RS232, SD/MMC, LCD, three status LEDs and two user buttons.

There are plenty of GPIOs on extension headers where you can connect your additional circuits.

## **BOARD FEATURES:**

- CPU: LPC2919FBD144 32 bit combine an ARM968E-S CPU core with two integrated TCM blocks operating at frequencies of up to 125 MHz, CAN and LIN, 56 kB SRAM, 768 kB flash memory, external memory interface, two 10-bit ADCs, and multiple serial and parallel interfaces in a single chip.

JTAG connector with ARM 2x10 pin layout for programming/debugging with ARM-JTAG, ARM-USB-OCD, ARM-USB-TINY

- RS232 port
- two CAN drivers and connectors
- two LIN drivers and connectors
- LCD 8X1
- SD/MMC card connector
- two user buttons
- trimpot connected to ADC
- RESET circuit
- RESET button
- three status LEDs
- power supply LED
- jumper for Power Selection mode
- three on board voltage regulators 1.8V, 3.3V and 5V with up to 800mA current
- single power supply: External power supply +9VDC required, or takes power from JTAG connector
- 16 Mhz crystal oscillator
- UEXT connector with SPI, RS232 and power supply for connecting add-on modules
- Extension port connector for many of microcontrollers pins
- Prototype area
- PCB: FR-4, 1.5 mm (0,062"), red soldermask, silkscreen component print
- Dimensions: 140x89mm (5.512x3.504")

## **ELECTROSTATIC WARNING:**

The LPC-P2919 board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

## **BOARD USE REQUIREMENTS:**

**Cables:** The cable you will need depends on the programmer/debugger you use. If you use [ARM-USB-OCD](#), you will need RS232 cable and 1.8 meter USB A-B cable and if you use [ARM-USB-TINY](#), you will need 1.8 meter USB A-B cable.

**Hardware:** Programmer/Debugger – one of the Olimex ARM Programmers: ARM-USB-OCD, ARM-USB-TINY.

**Software:** ARM C compiler and JTAG programmer, the possible options are:

- open source platform: GNU C compiler + OpenOCD and Eclipse

## **PROCESSOR FEATURES:**

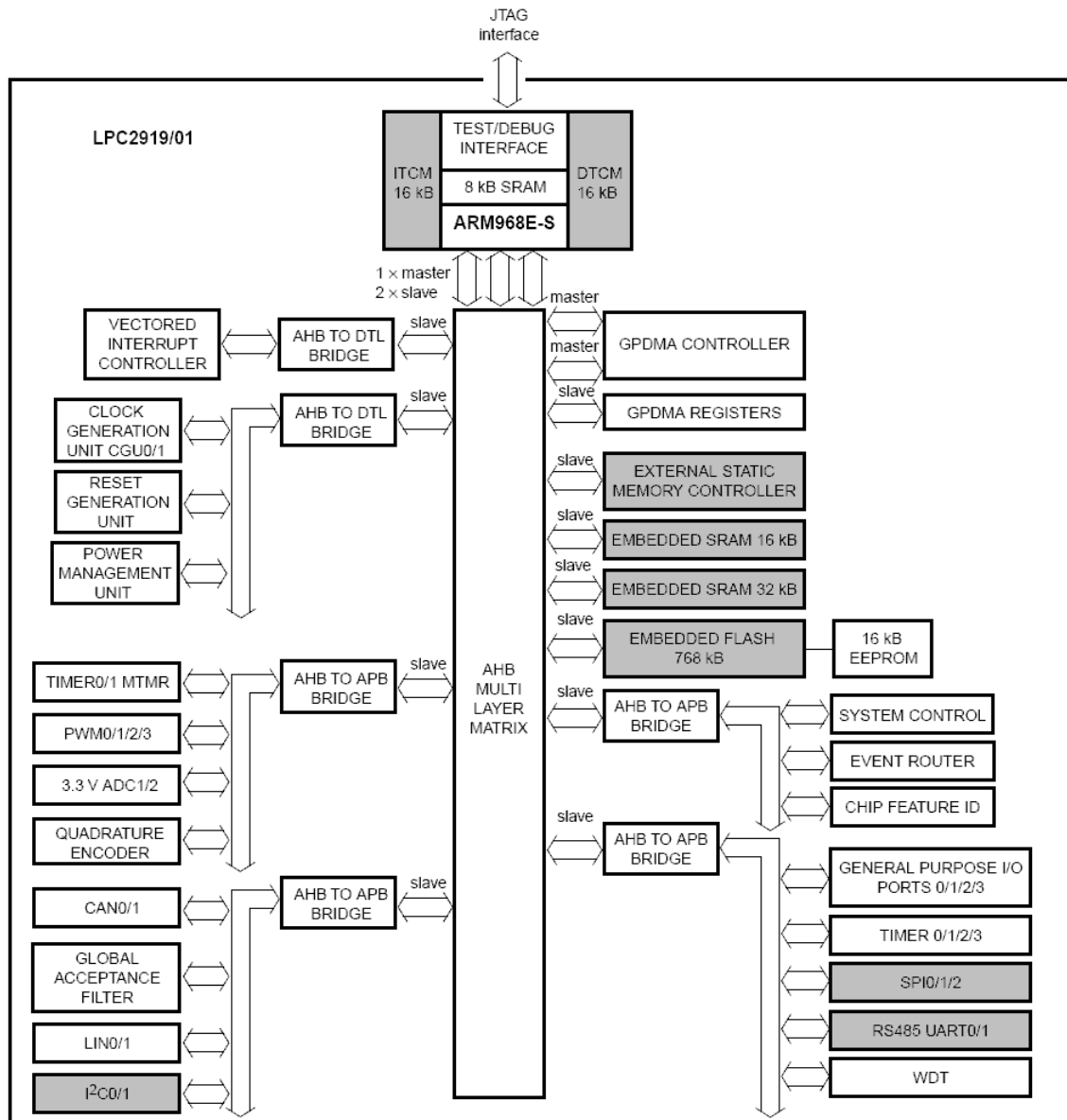
**LPC-P2919** board use ARM9 32-bit microcontroller **LPC2919FBD144** from NXP Semiconductors with these features:

- ARM968E-S processor running at frequencies of up to 125 MHz maximum.
- Multi-layer AHB system bus at 125 MHz with three separate layers.
- On-chip memory:
  - Two Tightly Coupled Memories (TCM), 16 kB Instruction (ITCM), 16 kB Data TCM(DTCM).
  - Two separate internal Static RAM (SRAM) instances; 32 kB SRAM and 16 kB SRAM.
  - 8 kB ETB SRAM also available for code execution and data.
  - 768 kB high-speed flash-program memory.
  - 16 kB true EEPROM, byte-erasable and programmable.
- Dual-master, eight-channel GPDMA controller on the AHB multilayer matrix which can be used with both I2C interfaces, the SPI interfaces, and the UARTs, as well as for memory-to-memory transfers including the TCM memories.
- External Static Memory Controller (SMC) with eight memory banks; up to 32-bit data bus; up to 24-bit address bus.
- Serial interfaces:
  - Two-channel CAN controller supporting Full-CAN and extensive message filtering.

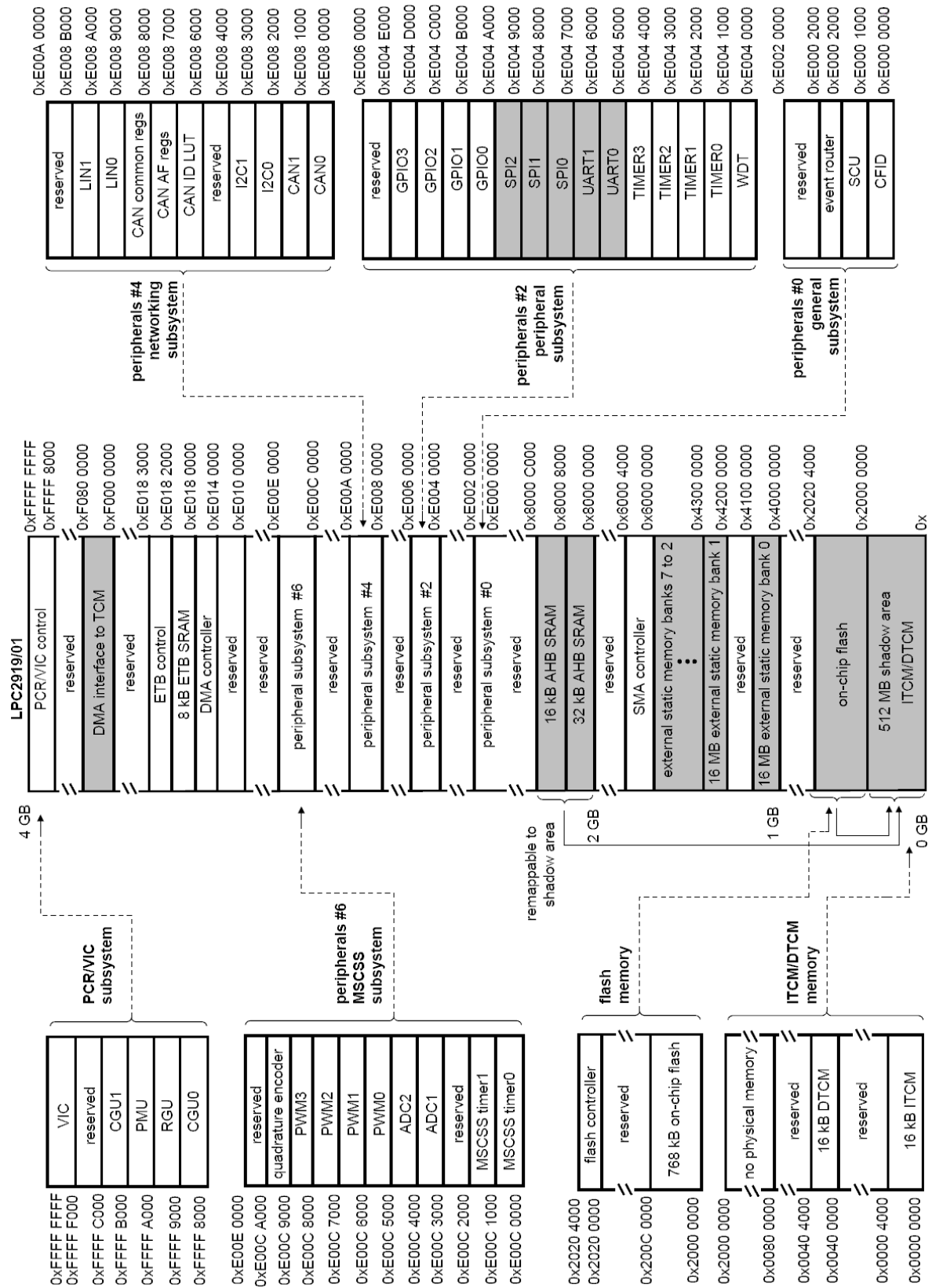
- Two LIN master controllers with full hardware support for LIN communication. The LIN interface can be configured as UART to provide two additional UART interfaces.
- Two 550 UARTs with 16-byte Tx and Rx FIFO depths, DMA support, and RS485 (9 bit) support.
- Three full-duplex Q-SPIs with four slave-select lines; 16 bits wide; 8 locations deep; Tx FIFO and Rx FIFO.
- Two I2C-bus interfaces.
- Other peripherals:
  - Two 10-bit ADCs, 8 channels each, with 3.3 V measurement range and conversion times as low as 2.44  $\mu$ s per channel. Each channel provides a compare function to minimize interrupts.
  - Multiple trigger-start option for all ADCs: timer, PWM, other ADC, and external signal input.
  - Four 32-bit timers each containing four capture-and-compare registers linked to I/Os.
  - Four six-channel PWMs (Pulse-Width Modulators) with capture and trap functionality.
  - Two dedicated 32-bit timers to schedule and synchronize PWM and ADC.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - 32-bit watchdog with timer change protection, running on safe clock.
- Up to 108 general-purpose I/O pins with programmable pull-up, pull-down, or bus keeper.
- Vectored Interrupt Controller (VIC) with 16 priority levels.
- Up to 19 level-sensitive external interrupt pins, including CAN and LIN wake-up features.
- Configurable clock-out pin for driving external system clocks.
- Processor wake-up from power-down via external interrupt pins; CAN or LIN activity.
- Flexible Reset Generator Unit (RGU) able to control resets of individual modules.
- Flexible Clock-Generation Unit (CGU0) able to control clock frequency of individual modules:
  - On-chip very low-power ring oscillator; fixed frequency of 0.4 MHz; always on to provide a Safe\_Clock source for system monitoring.
  - On-chip crystal oscillator with a recommended operating range from 10 MHz to 25 MHz. PLL input range 10 MHz to 25 MHz.
  - On-chip PLL allows CPU operation up to a maximum CPU rate of 125 MHz.
  - Generation of up to 11 base clocks.
  - Seven fractional dividers.

- Second CGU (CGU1) with its own PLL generates a configurable clock output.
- Highly configurable system Power Management Unit (PMU):
  - clock control of individual modules.
  - allows minimization of system operating power consumption in any configuration.
- Standard ARM test and debug interface with real-time in-circuit emulator.
- Boundary-scan test supported.
- ETM/ETB debug functions with 8 kB of dedicated SRAM also accessible for application code and data storage.
- Dual power supply:
  - CPU operating voltage: 1.8 V  $\pm$  5 %.
  - I/O operating voltage: 2.7 V to 3.6 V; inputs tolerant up to 5.5 V.
- 144-pin LQFP package.
- -40 °C to +85 °C ambient operating temperature range.

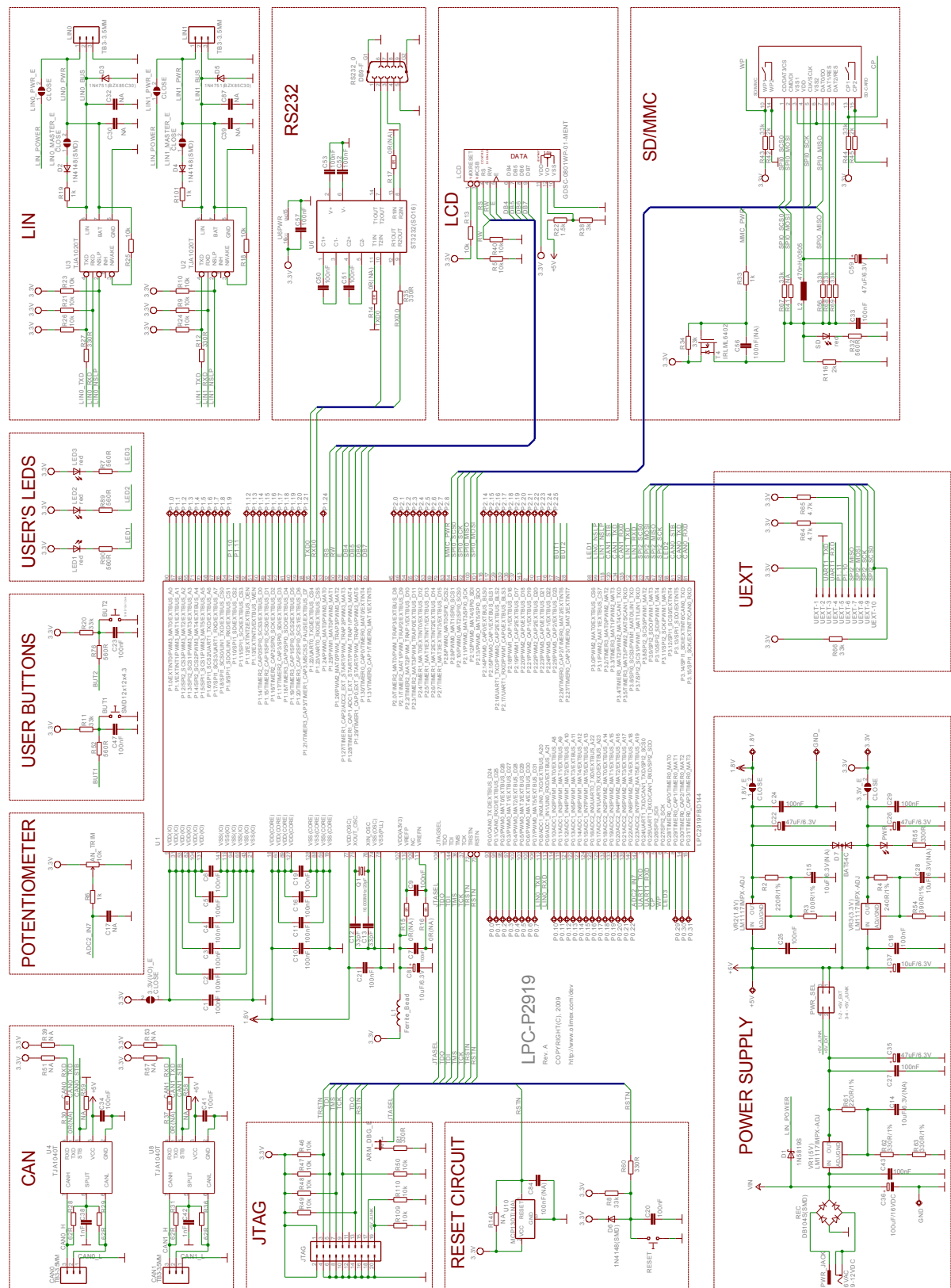
## Block Diagram:



# MEMORY MAP:

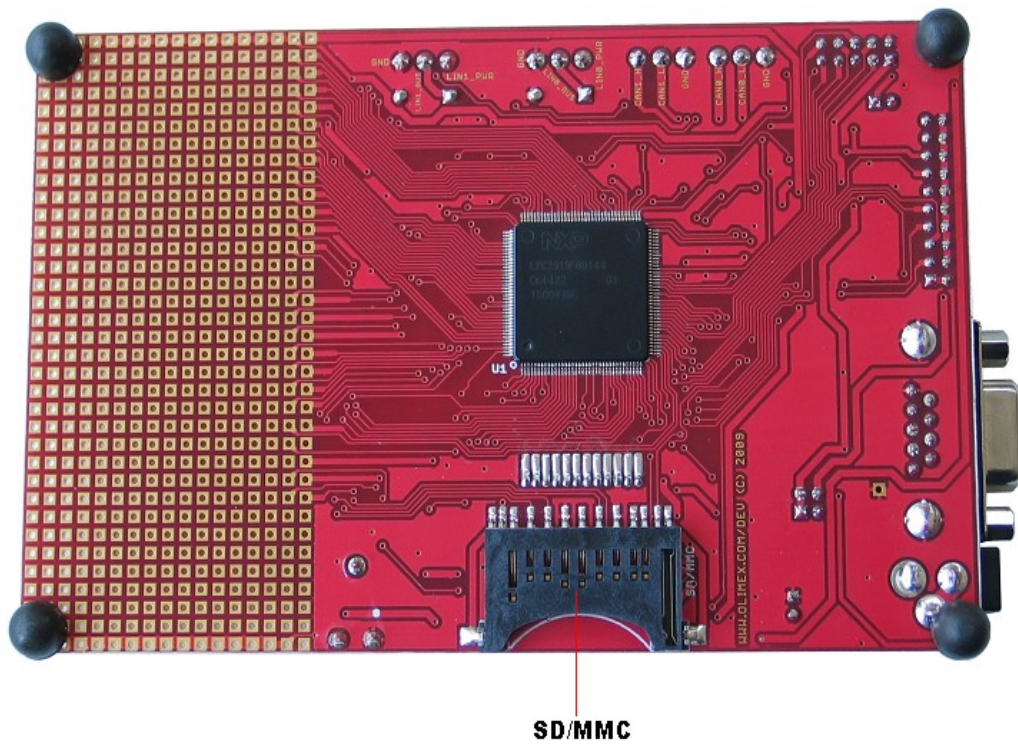
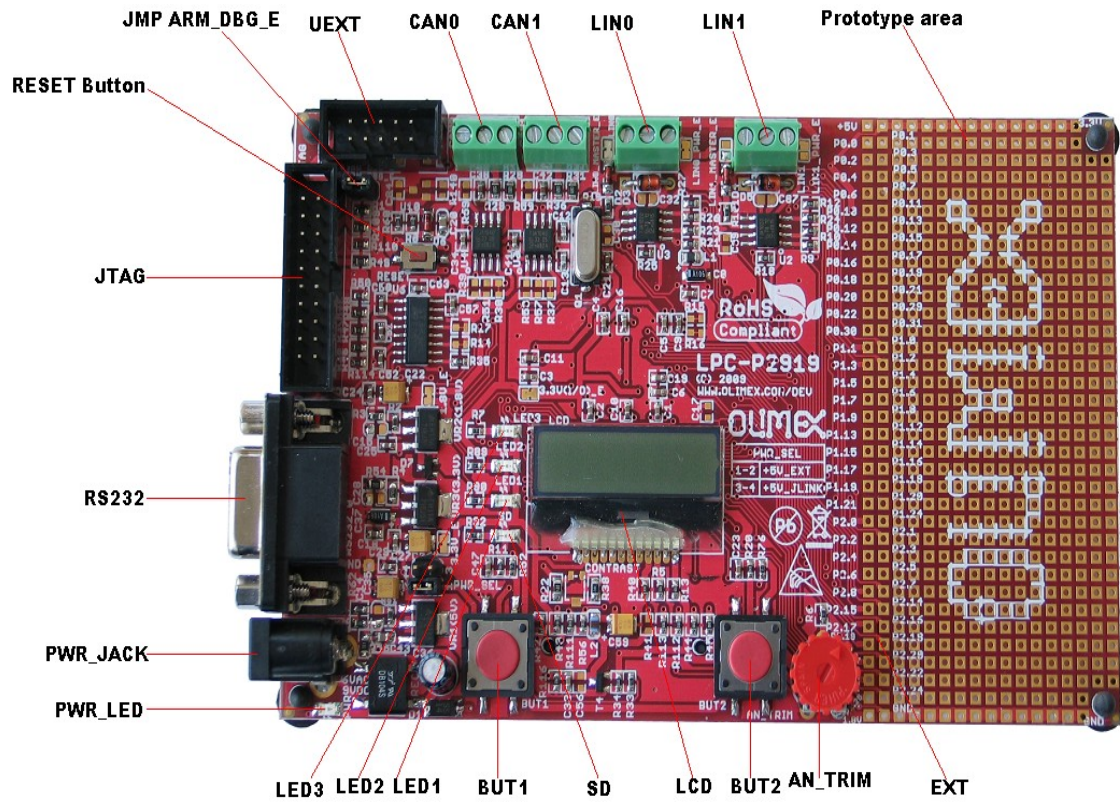


# SCHEMATIC





## BOARD LAYOUT



## POWER SUPPLY CIRCUIT

LPC-P2919 can take power from two sources:

- External power supply 9.0-12.0 V DC or 6.0V AC.
- +5V\_JLINK from JTAG connector

## RESET CIRCUIT

LPC-P2919 reset circuit includes pin 15 of JTAG connector, pin 73 of U1 and RESET button.

## CLOCK CIRCUIT

Quartz crystal 16 MHz is connected to LPC-P2919 pin 75 (XOUT\_OSC) and pin 76 (XIN\_OSC).

## JUMPER DESCRIPTION

### PWR\_SEL



When 1-2 are shorted – the board is supplied from PWR\_JACK, when 3-4 are shorted – the board is supplied from JTAG.

Default state is 1-2.

### ARM\_DBG\_E



When this jumper is shorted – selects the ARM debug mode; when it is open – selects boundary scan and flash programming; pulled up internally.

Default state is closed.

### LIN0\_MASTER\_E



Enable LIN0 master's pull-up.

Default state is closed.

### LIN0\_PWR\_E



Enable power supply to LIN0.

Default state is closed.

### LIN1\_MASTER\_E



Enable LIN1 master's pull-up.

Default state is closed.

### LIN1\_PWR\_E



Enable power supply to LIN1.

Default state is closed.

### 3.3V(I/O)\_E



Connects 6 pins (VDD(IO)) of LPC2919 to 3.3V.

Default state is closed.

### 1.8V\_E



Enable regulator VR2(1.8V) – LM1117

Default state is closed.

### 3.3V\_E



Enable regulator VR3(3.3V) – LM1117

Default state is closed.

## INPUT/OUTPUT

**SD/MMC LED (red)** with name **SD** connected to SD/MMC pin 4.

**Status LED1 (red)** with name **LED1** connected to LPC2919 pin 98 (P3.0/PWM2\_MAT0/EXTBUS\_CS6).

**Status LED2 (red)** with name **LED2** connected to LPC2919 pin 58 (P3.12/SPI1\_SCS0/EXTINT4).

**Status LED3 (red)** with name **LED3** connected to LPC2919 pin 7 (P0.28/TIMER0\_CAP0/TIMER0\_MAT0).

**Power-on LED (red)** with name **PWR** – this led shows that +3.3V is applied to the board.

**User button** with name **BUT1** connected to LPC2919 pin 27 (P2.26/TIMER0\_CAP2/TIMER0\_MAT2/EXTINT6).

**User button** with name **BUT2** connected to LPC2919 pin 28 (P2.27/TIMER0\_CAP3/TIMER0\_MAT3/EXTINT7).

**Reset button** with name **RESET** connected to LPC2919 pin 73 (RSTN).

**Trimpot** with name **AN\_TRIM** connected to LPC2919 pin 142 (P0.23/ADC2\_IN7/PWM2\_MAT5/EXTBUS\_A19).

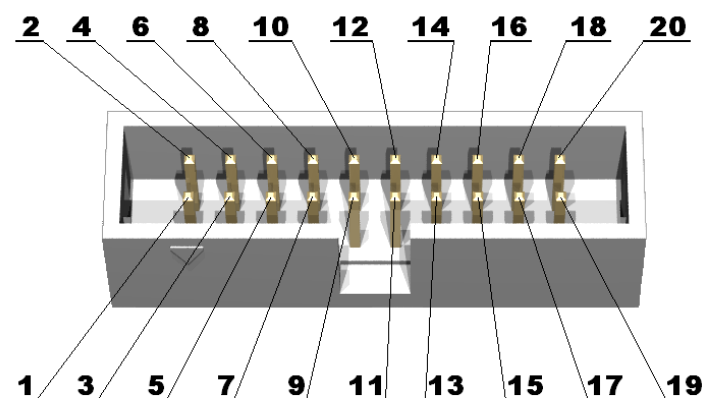
**LCD 8X1**

## CONNECTOR DESCRIPTIONS

### JTAG:

The JTAG connector allows the software debugger to talk via a JTAG (Joint Test Action Group) port directly to the core. Instructions may be inserted and executed by the core thus allowing LPC2919 memory to be programmed with code and executed step by step by the host software.

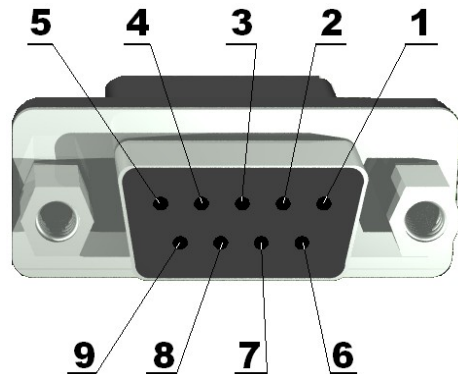
For more details refer to IEEE Standard 1149.1 - 1990 Standard Test Access Port and Boundary Scan Architecture and LPC2919 datasheets and users manual.



Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	3.3V
3	TRSTN	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	NC	12	GND
13	TDO	14	GND
15	RSTN	16	GND
17	PULL-DOWN	18	GND
19	+5V_JLINK	20	GND

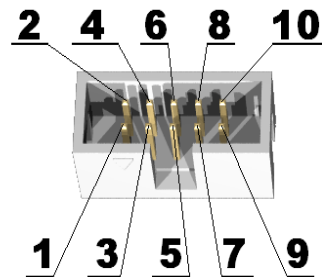
### RS232:

Pin #	Signal Name
1	NC
2	T2OUT
3	R2IN
4	NC
5	GND
6	NC
7	NC
8	NC
9	NC



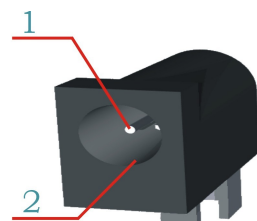
### UEXT:

Pin #	Signal Name
1	3.3V
2	GND
3	UART1_TXD
4	UART1_RXD
5	P1.11
6	P1.10
7	SPI2_MISO
8	SPI2_MOSI
9	SPI2_SCK
10	SPI2_SCS0



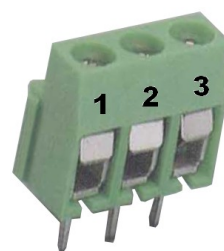
### PWR JACK:

Pin #	Signal Name
1	Power Input
2	GND



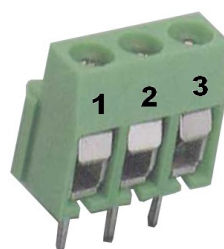
### CAN0:

Pin#	Signal	Description
1	GND	Ground
2	CAN0_L	CAN LOW
3	CAN0_H	CAN HIGH



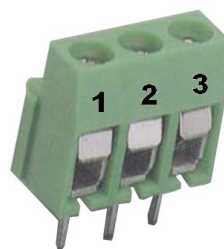
### CAN1:

Pin#	Signal	Description
1	GND	Ground
2	CAN1_L	CAN LOW
3	CAN1_H	CAN HIGH



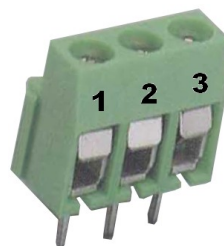
### LIN0:

Pin#	Signal	Description
1	LIN0_PWR	LIN Power
2	LIN0_BUS	LIN
3	GND	Ground

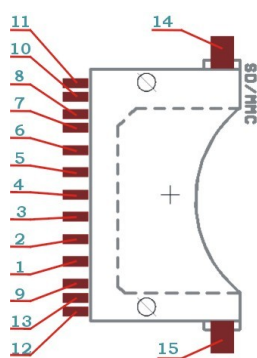


### LIN1:

Pin#	Signal	Description
1	LIN1_PWR	LIN Power
2	LIN1_BUS	LIN
3	GND	Ground



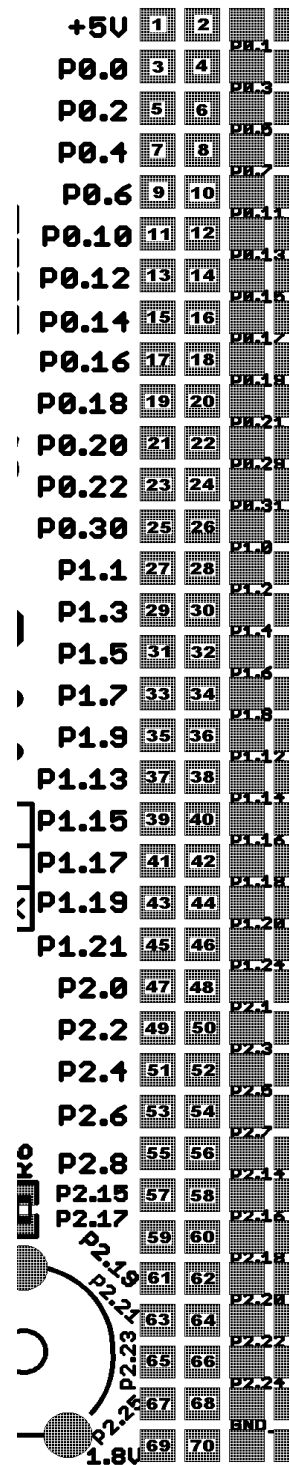
## SD/MMC



Pin #	Signal Name	Pin #	Signal Name
1	SPI0_SCS0	9	MCIDAT2
2	SPI0_MOSI	10	WP1
3	GND	11	NC
4	3.3V	12	NC
5	SPI0_SCK	13	CP1
6	GND	14	WP2
7	SPI0_MISO	15	CP2
8	MCIDAT1		

## EXT

Pin #	Signal Name	Pin #	Signal Name
1	+5V	2	+3.3V
3	P0.0	4	P0.1
5	P0.2	6	P0.3
7	P0.4	8	P0.5
9	P0.6	10	P0.7
11	P0.10	12	P0.11
13	P0.12	14	P0.13
15	P0.14	16	P0.15
17	P0.16	18	P0.17
19	P0.18	20	P0.19
21	P0.20	22	P0.21
23	P0.22	24	P0.29
25	P0.30	26	P0.31
27	P1.1	28	P1.0
29	P1.3	30	P1.2
31	P1.5	32	P1.4
33	P1.7	34	P1.6
35	P1.9	36	P1.8
37	P1.13	38	P1.13
39	P1.15	40	P1.14
41	P1.17	42	P1.16
43	P1.19	44	P1.18
45	P1.21	46	P1.20
47	P2.0	48	P1.24
49	P2.2	50	P2.1
51	P2.4	52	P2.3
53	P2.6	54	P2.5
55	P2.8	56	P2.7
57	P2.15	58	P2.14
59	P2.17	60	P2.16
61	P2.19	62	P2.18
63	P2.21	64	P2.20
65	P2.23	66	P2.22
67	P2.25	68	P2.24
69	+1.8V	70	GND



## I2C

The LPC2919 contain two I<sup>2</sup>C-bus controllers.



The I<sup>2</sup>C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device or as a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I<sup>2</sup>C is a multi-master bus, and it can be controlled by more than one bus master connected to it.

The main features of the I<sup>2</sup>C-bus interfaces are:

- I<sup>2</sup>C0 and I<sup>2</sup>C1 use standard I/O pins with bit rates of up to 400 kbit/s (Fast I<sup>2</sup>C-bus) and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- All I<sup>2</sup>C-bus controllers support multiple address recognition and a bus monitor mode.

## SPI

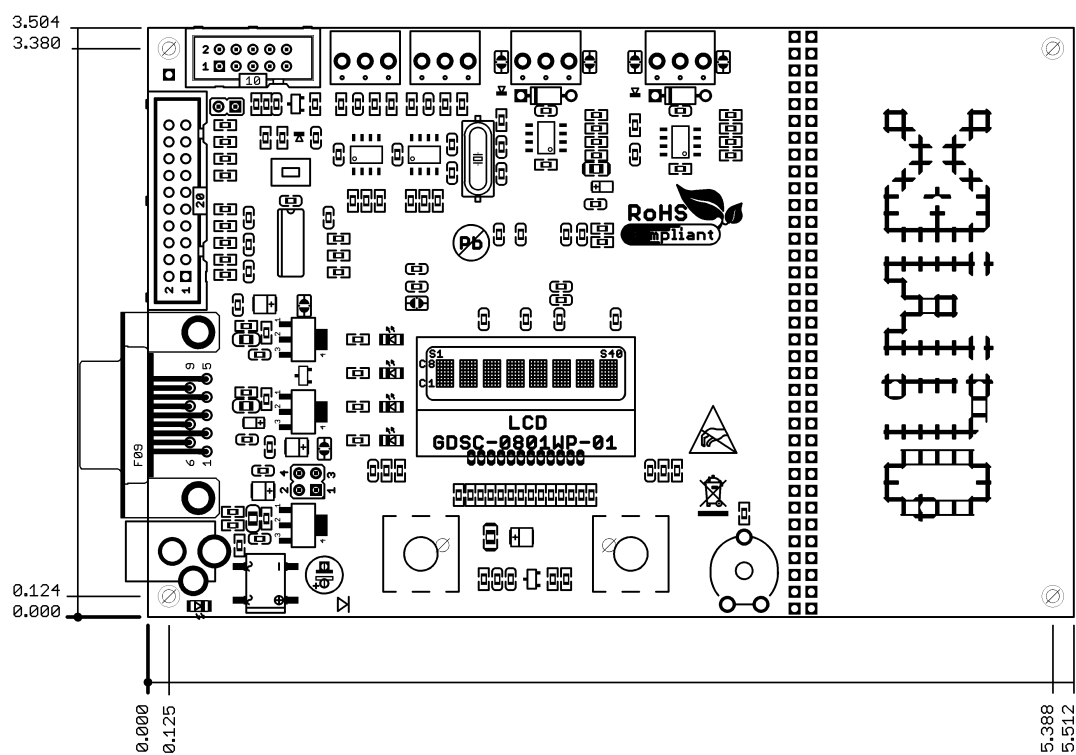
The LPC2919 contains three Serial Peripheral Interface modules (SPIs) to allow synchronous serial communication with slave or master peripherals.

The key features are:

- Master or slave operation.
- Each SPI supports up to four slaves in sequential multi-slave operation.
- Supports timer-triggered operation.
- Programmable clock bit rate and prescale based on SPI source clock (BASE\_SPI\_CLK), independent of system clock.
- Separate transmit and receive FIFO memory buffers; 16 bits wide, 32 locations deep.
- Programmable choice of interface operation: Motorola SPI or Texas Instruments Synchronous Serial Interfaces.
- Programmable data-frame size from 4 to 16 bits.
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts.
- Serial clock-rate master mode:  $f_{\text{serial\_clk}} \leq f_{\text{CLK(SPI)}}/2$ .
- Serial clock-rate slave mode:  $f_{\text{serial\_clk}} = f_{\text{CLK(SPI)}}/4$ .

- Internal loopback test mode.  
The SPI module can operate in:
- Master mode:
  - Normal transmission mode.
  - Sequential slave mode.
- Slave mode.

## MECHANICAL DIMENSIONS



All measures are in inches.

## **AVAILABLE DEMO SOFTWARE**

- Buttons and LCD demo
- Port\_LCD\_UART demo
- SD slot demo

## **ORDER CODE**

**LPC-P2919** – assembled and tested (no kit, no soldering required)

How to order?

You can order to us directly or by any of our distributors.

Check our web [www.olimex.com/dev](http://www.olimex.com/dev) for more info.

### **Revision history:**

REV.A                      - create    October 2009

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