INTEGRATED CIRCUITS

ERRATA SHEET

Date: 2007 May 23
Document Release: Version 1.0
Device Affected: LPC2888

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2007 May 23



Document revision history

| Rev | Date | Description |
|-----|--------------|---------------|
| 1.0 | May 23, 2007 | First version |

Identification

The typical LPC2888 devices have the following top-side marking:

LPC2888xxx

XXXXXX

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2888:

| Revision Identifier (R) | Comment |
|-------------------------|-------------------------|
| '-' | Initial device revision |

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

| Functional Problem | Short Description | Device Revision |
|-----------------------|---|-----------------|
| MCI.1 | Rx FIFO is not functional | - |
| Core.1 | Thumb code execution is not possible from on-chip 1MB Flash | - |

Errata Overview - AC/DC Deviations

| AC/DC Deviation | Short Description | Device Revision |
|--------------------|-------------------|-----------------|
| | | |

Errata Notes

| Note | Short Description |
|------|-------------------|
| NA | NA |

Functional Deviations of LPC2888

MCI.1: Rx FIFO is not functional

Introduction: The MCI block has a 16 word deep, 32 bits wide FIFO for incoming data. A total of 64 bytes can be

buffered before they must be read by the CPU or the DMA controller. The FIFO is always in the

data path, and cannot be disabled.

Problem: A read access to the MCI FIFO correctly returns the top word from the FIFO. However, every read

access (either by CPU or by the DMA controller) also takes a second word from FIFO, and this word is lost. Hence, DMA cannot be used with the MCI RX FIFO, because DMA transfers are only

requested once the MCI FIFO is half full.

Workaround: Every incoming word should be read from the MCI FIFO, before a second word arrives. A read

access to the MCI FIFO will then return that particular word. The undesired second read access will be a dummy read on an empty FIFO, and no data is lost. This can be achieved by using the 'RxDataAvlbl' condition which causes an interrupt as soon as new word is present in the FIFO. Once the interrupt fires, software should immediately read the FIFO before the next word arrives.

Core.1: Thumb code execution is not possible from on-chip 1MB Flash

Introduction: The LPC288x has an ARMTDMI core and it supports the Thumb Instruction set.

Problem: Thumb code cannot execute from on-chip Flash and if attempted, there will be a data abort

exception.

Workaround: No known workaround. Only ARM code execution is possible from the on-chip Flash.

Electrical and Timing Specification Deviations of LPC2888

No known electrical and timing deviations.

Errata Notes

No known Errata Notes