High Quality Professional Instruments




ZEROPLUS

ZEROPLUS

www.zeroplus.com.tw

In November, 1997, Zeroplus Technology Co., Ltd. was established by a group of engineers who have years of experience in MCU programming. ZEROPLUS possesses the core technology in IC Design. The advantages of the company come from deeply understanding the industry. Besides our know how, we have great passions in servicing customers and developing advanced products to meet trends of needs from the markets.

In 2004, the fields of business were extended to the electronic measurement instruments. Applying the advanced MCU programming technology, the company successfully developed the latest patented measurement instrument – PC-Based Logic Analyzer. Our unique and innovative products were designed according to the combination of many patents. As of June, 2009, the number of patent application has reached 216, 11 of which are about PCT. Our technologies are patents in many countries such as China, Japan, Canada, Taiwan, India, France, America, England, Singapore, Italy, Germany, and Korea. 132 of them belong to PI and 84 are UM. So far, we are patenting our technology in more and more countries.

Green Industry · Quality Products

All the products of ZEROPLUS have been certified to meet the regulations of safety such as the FCC Certificate of Compliance, the CE Certificate of Compliance, the test of EMI, EMC, ESD of the Bureau of Standards, Metrology and Inspection Ministry of Economic Affairs and so on. Our excellent qualities satisfying the strict Environment Estimation Test from the Electronics Inspection Center, Taiwan with conditions as below: High and Low Temperature (-40˚C~+80˚C), 95% RH, 70˚C high temperature and high humidity test, Drop Test with the bare product and the certification with 200MHz Sampling Frequency. To be a responsible company protecting environment, our products are qualified meeting the regulations of RoHS and WEEE. Customers could always trust our products.

Innovative vision and a superior brand - the honored Taiwan Excellence Award

ZEROPLUS participated in the competition of Taiwan Excellence Aword. Our self-developed Logic Analyzers won the prizes of Taiwan Excellence Award 2006 and 2009. Our R & D technology, quality management, marketing and brand name have been well recognized nationally and internationally.

Worth To Own - ZEROPLUS Logic Analyzer

"High Quality Professional Instruments" is the core value of ZEROPLUS. In order to provide customers with excellent quality products, we are insistent innovating manufacture processes . We are proud of our Logic Analyzer which is worth to own by every engineer. It can reduce the development time and cost, but enhance the quality of your projects effectively. Our Logic Analyzer is the best tool to assist researchers, students, and SOHO workers in the filed of electronics as well as the indispensable teaching material for electronic educational institutions.

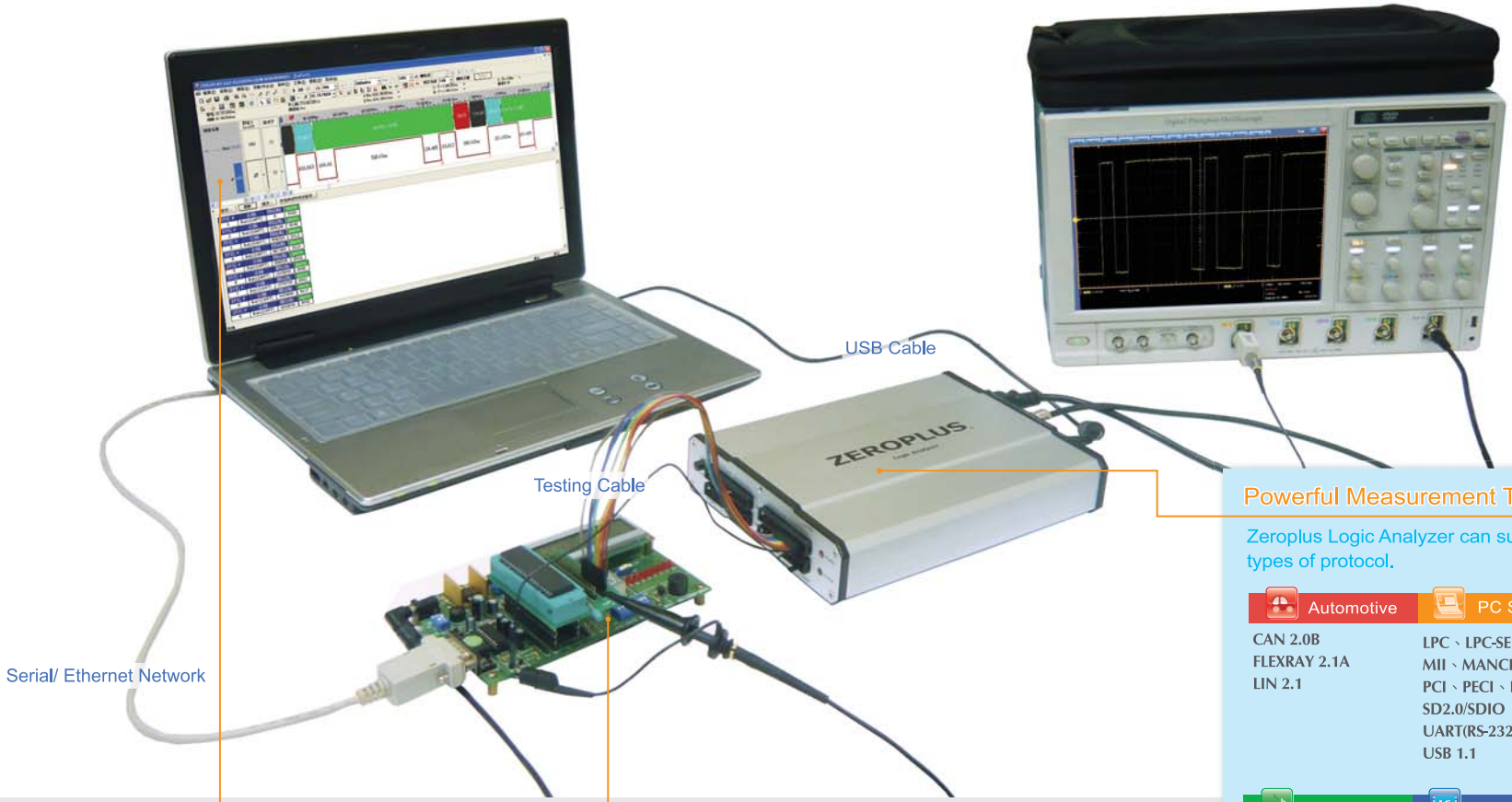
Patent Certification

Safety Certification

RoHS SVHC

What is Logic Analyzer?

Logic Analyzer is used to test digital signals, which is similar to the Oscilloscope but detecting the high/low status of digital signals. Logic Analyzer isn't only detecting logic status but also store and display them on computers. The users could study data as wave form or status form which timing stamp is displayed. It is very useful tool debugging sequntial circuit design (Hardware Design and Firmware Design). Logic Analyzer is able to observe signals from 8 channels or more at the same time (oscilloscope is only to observe 2 channels or 4 channels at same time) and calculating bus figures, so it plays an important role in steps of electronics design and research and development. Its function is very powerful. Users can analyze the error and solve the question quickly then using oscilloscope.



Powerful Measurement Tools

Zeroplus Logic Analyzer can support and analyze many types of protocol.

Automotive

CAN 2.0B
FLEXRAY 2.1A
LIN 2.1

PC System

LPC、LPC-SERIRQ
MII、MANCHESTER
PCI、PECI、PS/2
SD2.0/SDIO
UART(RS-232C/422/485)
USB 1.1

Memory

1-WIRE、3-WIRE
I2C
I2C(EEPROM 24LX)
ISO7816 UART
SPI、SPI PLUS、SLE4442
UNI/O

Digital Audio

AC97、HDA、IIS
PCM、S/PDIF、ST

IC Interface

JTAG 2.0
MICROWIRE
MCU-51 DECODE
SSI

Basic Logic Application

ARITHMETIC LOGIC
DIGITAL LOGIC
JK FLIP-FLOP
UP DOWN COUNTER

Other

7-SEGMENT LED、CCIR656、DALI、DIGRF、DSA、DMX512、HDQ、IRDA
LCD12864、LCD1602、MILLER、MOD、MODIFIED MILLER
MODIFIED SPI、PM 1.1、PSB、SDQ、SIGNIA 6210、SM2.0、ST7669
NEC PD6122、WIEGAND

Host System

Integrated Circuit Device
(Integrated Development Environment)

- Compiler
- Assembly Language Program
- Connector

Suitable for :

- Electronic Hardware/ Software/ Professional Development Tool Design of the Firmware Design.
- Development Tools for the Microcontroller, such as PICXX/8051/ARMx/ Renesas/Freescale etc...
- FPGA/CPLD Development Tool.
- Development Tools of other Prototype Digital Systems

How to select an ideal Logic Analyzer?

Test Channels

Most PC-Based Logic Analyzers have more than 2 capture channels. The ZEROPLUS advanced PC-Based Logic Analyzer B-series has more than 64 channels, enabling it to measure PCI protocol (47pins) or MCU51 code decoding (18 pins).

Capture Memory

The RAM Size determines the length of recorded signal capture. ZEROPLUS has been granted several patents for the innovation of Trigger Pages, Data Compression, Capture Filtering and Capture Memory Upgrade capability .

Data Pages:
Long data captures can be displayed as pages (page mode) to simplify display. Pages can be selected like reading a book.

Data Compression:
ZEROPLUS incorporate a sophisticated compression algorithm, optimising the use of capture memory and enabling more data to be captured without loss of any information.

Filtering:
Captured data may be filtered before being saved in the Capture Memory. This allows the user to store only the data they need.

Memory \ Sampling Frequency	50MHz	100MHz	200MHz	333MHz	500MHz	1GHz
128K	2.621ms	1.311ms	655.36us	393.609us	262.144us	131.072us
256K	5.243ms	2.621ms	1.311ms	787.219us	524.288us	262.144us
1M	20.972ms	10.486ms	5.243ms	3.1488ms	2.097ms	1.048ms
2M	41.943ms	20.972ms	10.486ms	6.297ms	4.194ms	2.097ms
4M	-	-	-	-	8.388ms	4.194ms
8M	-	-	-	-	-	8.388ms

▲ Comparison Table of Time of Signals

Sampling Frequency

Similar to the RAM Size, the higher the Sampling frequency, the higher the test precision. We suggest a sampling frequency of at least 4 times the signal frequency to capture your signal.

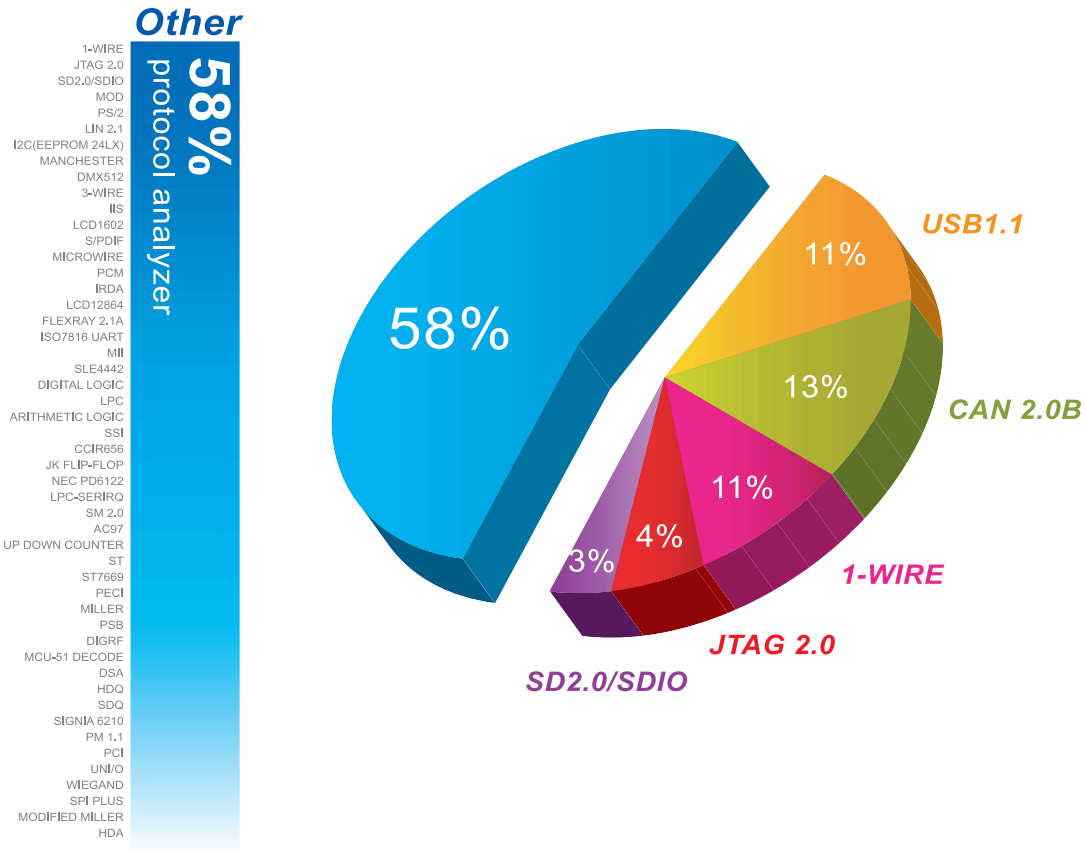
Feature-rich Software

The new version features over 80 functions and patented features including Waveform Zoom, Data Width Automatic Demonstration Mode, Fast Demonstration Full Page Pattern Mode and Data Comparison Demonstration Mode.

Differential Advantage

According to ZEROPLUS 2008~2009 global protocol statistics, IIC, UART, SPI, CAN and USB are the most popular protocols but these tops could only meet 42% market share. It means other 58% users are still looking for professional debug solution of other protocols.

ZEROPLUS logic analyzer devotes variety protocols and features over 56 different bus protocols from multi-media, automative, memory and PC system to content all market requirement.
We also provide free customized protocol developing service and release SDK (Software Development Kit) for engineers to design their own protocols.

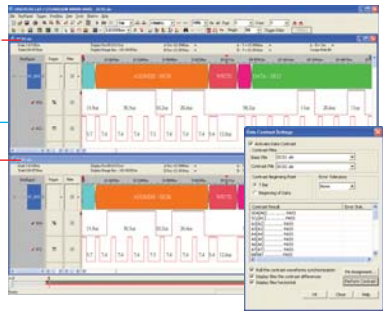


▲ Over 56 protocols from multi-media, automative, memory and PC system to content all market requirement.

Features & Interface

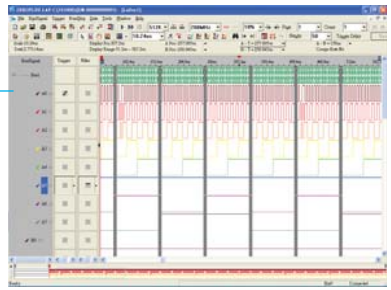
Data Contrast

According to the captured data, the Data Contrast can be used to analyze the contrasted results and mark the difference between the two files on the waveform display area.



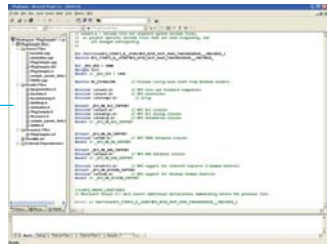
Filtration

Captured data may be filtered before being saved in the Capture Memory. This allows the user to store only the data they need.

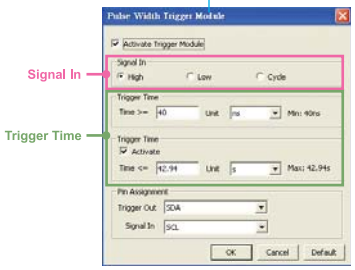


SDK (Software Development Kit)

ZEROPLUS pushes out SDK, including SDK for Protocol Analyzer, SDK for Date Contrast, etc., which can compile the Protocol Analyzer and Data Contrast by using the C Programming Language Development Environment. Engineers can modify and design them according to their requirements.



Pulse Width Trigger Module



Condition 1 : Signal In

3 selectable trigger modes : high level ,low level ,and wave form cycle mode.

Condition 2 : Trigger Time

Minimum and maxium setting range : 40ns ~ 42.94sec.

Protocol Analyzer Modules

It has provided more than fifty Protocol Analyzer Modules, such as IIC, UART, SPI, 1-WIRE, HDQ, CAN2.0B, USB1.1 and so on, relating to the Multimedia, the Computer Peripherals, the IC Interface and the Memory, etc.. And they all own the human.

Operating Systems

Windows 2000/XP/Vista

Statistics

Positive Period/ Full Period/ users can set the conditions according to their requirements.

Packet List

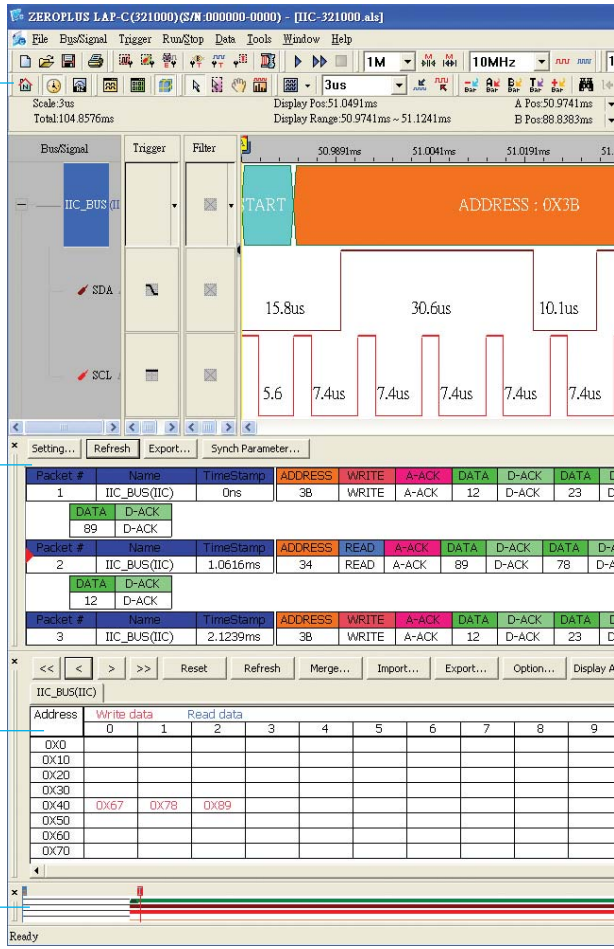
When analyzing the Protocol Analyzer, users can analyze the packet of the Protocol Analyzer. It will display the packet list horizontally, and it helps to analyze the decoded packets.

Memory Analyer

This function is mainly for the Protocol Analyzer with the ADDRESS, such as IIC, HDQ, 3-WIRE, PM, SM, IIC (EEPROM 24LX) and so on. It can record the statuses of the ADDRESS, READ/WRITE, DATA in the list of Memory Analyzer, which can make users record and analyze the ADDRESS, READ/WRITE and DATA when they analyze the Protocol Analyzer.

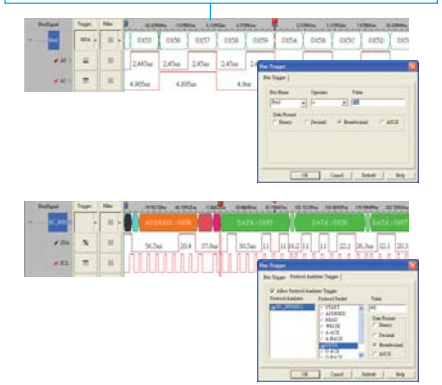
Navigator for Waveform

This function is mainly for keeping pace with the waveform in the selected area of the Navigator. When users move the waveform and some data has been changed, the Navigator will do the corresponding change.



Set Trigger Condition

User defined trigger condition and setting mode in both serial signal and parallel signal.



Multi-stacked Logic Analyzer Settings

This function means that it can connect many Logic Analyzers of the LAP-C Series. In this way, it can increase the RAM Size or the number of the Channel; users can connect four Logic Analyzers at most. (not supported under 162000 models)

Logic Cube Max. Four Units

Memory mode : LAP-C(32128) + LAP-C(32128)

Memory=256K, Channel=31CH

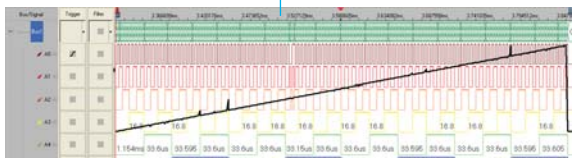
Channel mode : LAP-C(322000) + LAP-C(322000)

Memory=2Mbits, Channel=62CH

Features & Interface

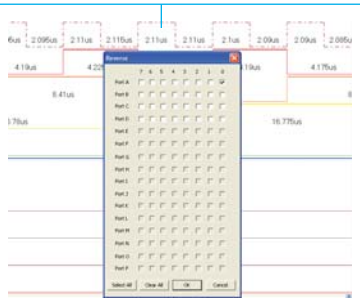
Analog Waveform

This function can display the value of each data by way of the curve mode on the waveform display area when users analyze the Protocol Analyzer, and users can judge that the data is correct or not according to the description of the Analog Waveform when they analyze the value of the Protocol Analyzer.



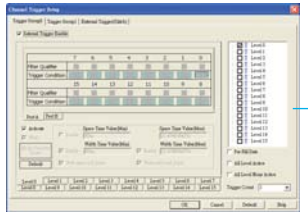
Reverse for Waveform

This function of Reverse is to reverse the collected signal. Change the High Level into the Low Level; change the Low Level into the High Level. The Reverse of Waveform Mode displays with the dashed, so it is easy to distinguish.



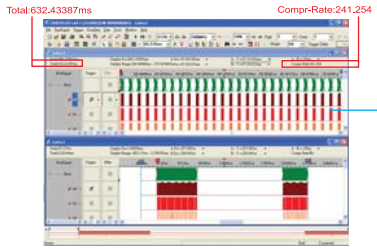
Multi-Level Trigger

The LAP-B Series provides three different Trigger functions: There are the Multi-Level Trigger, Pulse Width Trigger and Space Time Trigger.



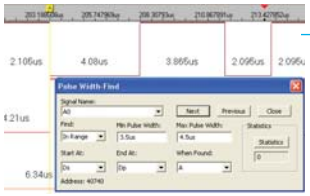
Data Compression

ZEROPLUS incorporate a sophisticated compression algorithm, optimising the use of capture memory and enabling more data to be captured without loss of any information.



Pulse Width- Find

It can compare and search the Pulse Width. For instance, the period of some Pulse Width is 4.2us (the positive/ negative period is 2.1us respectively), but it will cause the period error sometimes; at that moment, engineers can use the function of Pulse Width- Find to mark the error point.

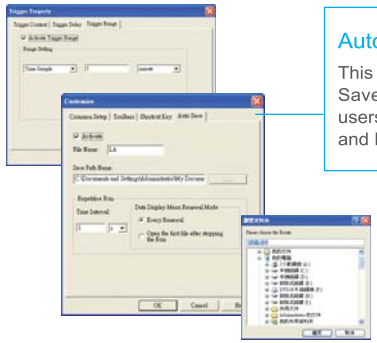


Synch Parameter Setting

Roll the Bar, and then the Packet List and the Waveform will be displayed synchronously.

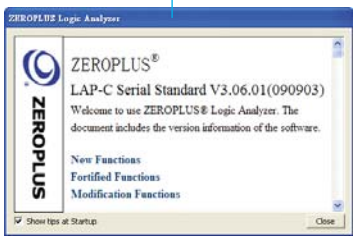
Auto Save

This function provides the user-defined Save Mode and selectable Mode for users, which includes the Time Sample and Frequency Sample.



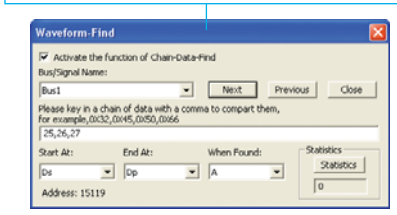
Software Version Information Display

The window display the current version of the software, the new functions or the modification status. It is convenient for users to learn the current version information of the software.



Chain-Data-Find

The original function of Find Data Value can only find one data, but the function of Chain-Data-Find enhances the Find function; for instance, the signal owns the chain data which are 0X01, 0X02, 0X03 ⋯0X25, 0X26, 0X27⋯0X40, then engineers can set the 0X25, 0X26 and 0X27 as the target of Find; it improves the efficiency of analyzing the signal.



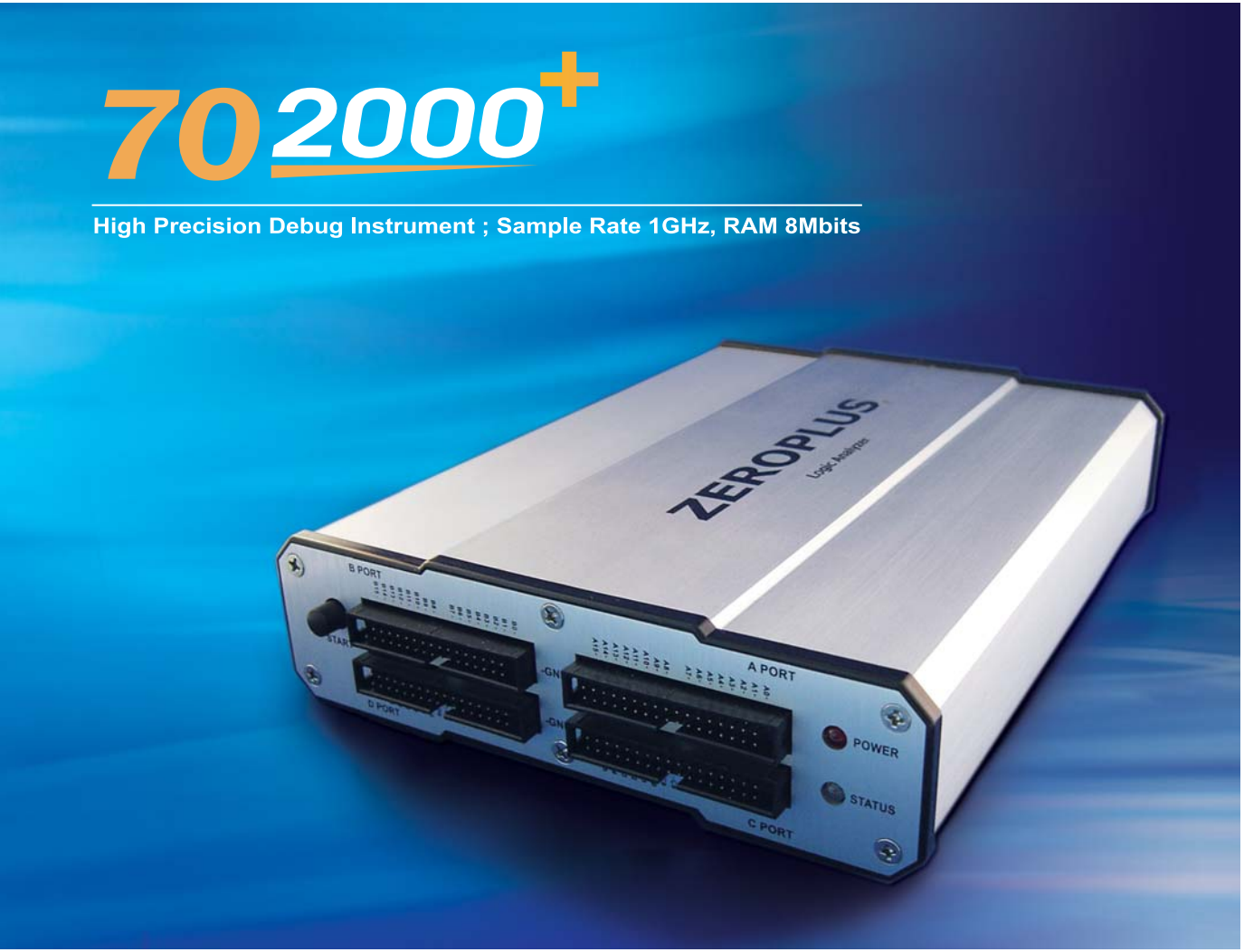
Export Waveform

It can convert the waveform into the TXT File and CVS File.

LAP-B (702000+)

High Quality Professional Instruments

PC-Based Logic Analyzer



- **USB2.0 (1.1) to transmit data:** It supports the full 480Mbps USB 2.0 speed.
- **Operating system:** Windows 2000/XP/Vista.
- **Multi-channel:** 70 channels, 2K~2Mbit RAM size per channel.
- **Sample Rate :** 1GHz, 8Mbits sampling. (only support 16CH mode)
- **Online Update:** automatic online software update.
- **Oscilloscope Connectivity:** LAP-B(702000+) has been designed to work with an oscilloscope to enable both analog and digital signals to be captured.
- **SDK (Software Development Kit):** C Programming Language Development Environment. Engineers can modify and design their individual protocol.
- **Feature-rich Software:** The new version features over 80 functions and patented features including Waveform Zoom, Data Width Automatic Demonstration Mode, Fast Demonstration Full Page Pattern Mode and Data Comparison Demonstration Mode.
- **Data Pages:** Long data captures can be displayed as pages (page mode) to simplify display. Pages can be selected like reading a book.
- **Data Compression:** ZEROPLUS incorporate a sophisticated compression algorithm, optimising the use of capture memory and enabling more data to be captured without loss of any information.
- **Filtration:** Captured data may be filtered before being saved in the Capture Memory. This allows the user to store only the data they need.
- **Protocol Analyzer:** Supply communication protocol I2C, UART, SPI, 1-WIRE, HDQ, CAN, USB1.1, I2S for analysis displaing in DATA BUS and PACKET LIST, new function continues to increase.

LAP-B (702000+)

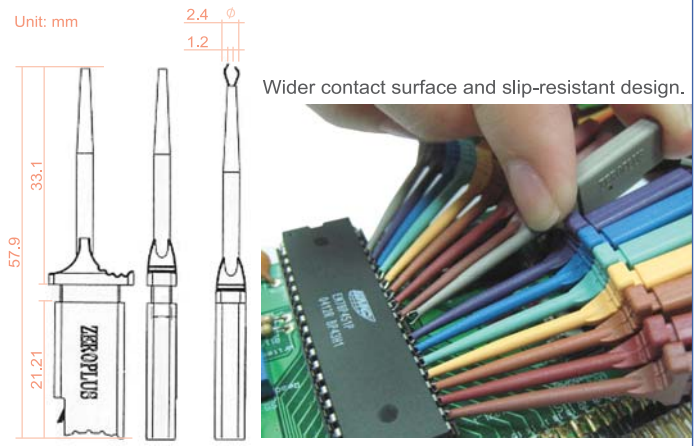
Product Model			LAP-B (702000+)		
Channel Mode			70CH Mode	32CH Mode	16CH Mode
Operating System			Windows 2000/XP/Vista		
Interface			USB2.0(1.1)		
Sample Rate	Internal Clock (Timing Mode)		100Hz~333MHz*	100MHz~500MHz	200MHz~1GHz
	External Clock (State Mode)		Max. 150MHz	N/A	N/A
	Mix Sampling Clock Fuction		✓		
Threshold Voltages	Bandwidth		150MHz		
	Working Range		-6V~+6V		
	Accuracy		±0.1V		
Memory	Memory		140Mbits		
	Depth (Per Channel)		2Mbits	4Mbits	8Mbits
Trigger	Condition	External	AND/OR/XOR/NOR/NAND/XNOR		
		Internal	Pattern/Edge/Pulse Width/AND/OR		
	Trigger Channel	External	3CH		
		Internal	64CH	32CH	16CH
	Pre/Post Trigger		N/A		
	Pulse Width Trigger		✓		
	Trigger Level		16 Level		
	Trigger Count		1~65535		
Software Functions	Data Compression (Per Channel)		Max. 1Mbits x 4G	N/A	N/A
	Filter & Filter Delay		✓	N/A	N/A
	Language		Chinese (Simplified/Traditional) / English		
	Time Base Range		5ps~10Ms		
	Vertical Sizing		1~5.5		
	Maximum Trigger Page		1~8192 Pages	1 Page	
	Waveform Data Display		✓		
	Unlimited Increasing Bar		✓		
	Automatic Attaching Bar		✓		
	Automatic Software Upgrade		✓		
	Selectable Analysis Range		✓		
	Data Statistic		✓		
	Auto-Save		✓		
	Filter Bar		✓		
	Protocol Analysis		✓		
	Data Contrast		✓		
	Latch Function		✓		
	Protocol Packet List		✓		
	File Export		✓		
	Protocol Packet Trigger		✓		
Protocol Analyzer Module (Free)			1-WIRE, 7-SEGMENT LED, CAN2.0B, HDQ, IIC, IIS, LIN 2.1, MANCHESTER, MICROWIRE, MILLER, PS/2, SPI, SSI, UART(RS-232C/422/485), USB1.1		
Protocol Analyzer Module (Option)			3-WIRE, AC97, ARITHMETIC LOGIC, CCIR656, DALI, DSA, DIGITAL LOGIC, DIGRF, DMX512, FLEXRAY 2.1A, I2C(EEPROM 24LX), IRDA, ISO7816 UART, LCD12864, LCD1602, LPC, LPC-SERIRQ, MCU-51DECODE, MII, MOD, MODIFIED MILLER, MODIFIED SPI, NEC PD6122, PCI, PCM, PECI, PM1.1, PSB, S/PDIF, SD2.0/SDIO, SDQ, SIGNIA 6210, SLE4442, SM2.0, SPI PLUS, ST, ST7669, JK FLIP-FLOP, JTAG 2.0, UNI/O, UP DOWN COUNTER, WIEGAND		
Phase Errors			<1.5ns		
Power			AC 110/220 V		
Maximum Input Voltage			±DC 30V		
Impedance			500KΩ/10pF		
Safety Certification			FCC/CE		

* When Sampling Frequencey > 200MHz , Compression and Filter function will be disable.

Standard Accessories

	Carry Bag		Test Cable 1-Pin *4 2-Pin *4 8-Pin *8
	Probe (Testing Hook) 36pcs *2	Probe (Testing Hook) 	BNC Cable
	AC Cable		USB Cable
	Installation Guide		Driver CD

Probe Specification



TAIWAN EXCELLENCE 2009

Taiwan External Trade Development Council

Logic Cube

PC-BASED LOGIC ANALYZER LAP-C SERIES

■ PC-Based interface

The ZEROPLUS logic has a Start button to commence sampling, and connects to a PC via fast USB v2.0 (v1.1 compatible) interface. 2000/XP/VISTA compatible.

■ Oscilloscope Connectivity

Logic Cube has been designed to work with an oscilloscope to enable both analog and digital signals to be captured.

■ Protocol Analyzer Module

ZEROPLUS features include the decoding of 54 different bus protocols from multi-media, automotive, IC interface, Memory to PC system and protocols including I2C, UART, SPI, 1-WIRE, CAN, etc. We can also provide customized protocol decoding.

■ Data Compression

The ZEROPLUS incorporates a sophisticated compression algorithm which enables more data to be captured without loss of any information.

■ Programmable Trigger

User defined trigger condition and setting mode in both serial signal, parallel signal and trigger delay functions.

■ Filtration

Captured data may be filtered to economise on capture memory. This allows the user to store only the data they need.

■ New Version

2009 new version features include waveform zoom, data width automatic demonstration mode, fast demonstration full page pattern mode, data comparison demonstration mode etc.

■ Extending Channel Capture

Logic analyzers may be linked to increase both capture memory and the number of channels. (32 Channel Series)

Logic Cube Max. Four Units

Channel mode: LAP-C(322000) + LAP-C(322000) =>
Channel = 62CH, Memory = 2Mbits

Memory mode: LAP-C(32128) + LAP-C(32128) =>
Channel = 31CH, Memory = 256Kbits

Logic Cube

Product model		LAP-C(16032)	LAP-C(16064)	LAP-C(16128)	LAP-C(162000)	LAP-C(32128)	LAP-C(321000)	LAP-C(322000)
Operating System		Windows 2000/XP/Vista						
Interface		USB2.0(1.1)						
Sample Rate	Internal Clock (Timing Mode)	100Hz~100MHz	100Hz~100MHz	100Hz~200MHz	100Hz~200MHz	100Hz~200MHz	100Hz~200MHz	100Hz~200MHz
	External Clock (State Mode)	75MHz	75MHz	100MHz	100MHz	100MHz	100MHz	100MHz
Threshold Voltages	Bandwidth	75MHz	75MHz	75MHz	75MHz	75MHz	75MHz	75MHz
	Working Range	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V
	Accuracy	±0.1V	±0.1V	±0.1V	±0.1V	±0.1V	±0.1V	±0.1V
Memory	Memory	512Kbits	1Mbits	4Mbits	64Mbits	4Mbits	32Mbits	64Mbits
	Depth (Per Channel)	32Kbits	64Kbits	128Kbits	2Mbits	128Kbits	1Mbits	2Mbits
Trigger	Condition	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge
	Trigger Channel	16CH	16CH	16CH	16CH	32CH	32CH	32CH
	Pre/Post Trigger	YES	YES	YES	YES	YES	YES	YES
	Trigger Level	1 Level	1 Level	1 Level	1 Level	1 Level	1 Level	1 Level
	Trigger Count	1~65535	1~65535	1~65535	1~65535	1~65535	1~65535	1~65535
Software Functions	Data Compression(Per Channel)	Max. 8Mbits	Max. 16Mbits	Max. 32Mbits	Max. 512Mbits	Max. 32Mbits	Max. 255Mbits	Max. 512Mbits
	Time Base Range	5ps~10Ms						
	Vertical Sizing	1~5.5						
	Language	Chinese (Traditional/Simplified) English						
	Maximum Trigger Page	8192 Pages						
	Waveform Data Display	✓						
	Filter & Filter Delay	✓						
	Trigger Delay	✓						
	Unlimited Increasing Bar	✓						
	Automatic Attaching Bar	✓						
	Automatic Software Upgrade	✓						
	Selectable Analysis Range	✓						
	Data Statistic	✓						
	Auto-Save	✓						
	Filter Bar	✓						
	Protocol Analysis	✓						
	Data Contrast	N/A			✓	N/A	✓	
	Latch Function	N/A			✓	N/A	✓	
	Protocol Packet List	✓						
	File Export	✓						
	Protocol Packet Trigger	parallel						serial、parallel
Pulse Width Trigger Module		Option						Free
Phase Errors		<1.5ns						
Power	Power	USB (DC 5V, 500mA)						
	Power at rest	1W						
	Power at work	2W						
Maximum Input Voltage		±30V						
Impedance		500KΩ/10pF						
Safety Certification		FCC / CE / WEEE / RoHS / SVHC						
Product Dimension		125mm*92mm*25mm						
Standard Accessories	Test Cable	8pin*2 / 2pin*1 / 1pin*1				16pin*1 / 8pin*2 / 2pin*1 / 1pin*1		
	Probe (Testing Hook)	2 pieces	20 pieces/package			36 pieces/package		
	USB Cable	1						
	Driver CD	1						
	Installation Guide	✕	1					
	Portable bag	✕	1					

Logic Cube Standard Accessories

Probe (Testing Hook)	
16CH (8pin*2 / 2pin*1 / 1pin*1) 32CH (16pin*1 / 8pin*2 / 2pin*1 / 1pin*1)	
Test Cable	16CH(20pcs) 32CH(36pcs)
USB Cable	1
Driver CD	1
Installation Guide	1
Portable Bag	1

Pulse Width Trigger Module (Option)

The additional pulse width trigger module could upgrade logic analyzer pulse width trigger capability.

- Pulse Width Trigger Module *1
- Test Cable (7pins)*1
- Test Cable (2pins)*1
- User Guide *1

5.4cm(L) * 4.5cm(W) * 1.8cm(H) 50g

RoHS SVHC

Protocol Analyzer

Automotive | PC System | Memory | Digital Audio | IC Interface | Basic Logic Application | Other

Product Model / Protocol Analyzer	LAP-B(702000+)	LAP-C(322000)	LAP-C(321000)	LAP-C(32128)	LAP-C(162000)	LAP-C(16128)	LAP-C(16064)	LAP-C(16032)
CAN 2.0B	free	free	free	support	free	support	support	support
FLEXRAY 2.1A	support	support	support	support	support	support	support	support
LIN 2.1	free	free	support	support	support	support	support	support
LPC	support	support	support	support	support	support	*	*
LPC-SERIRQ	support	support	support	support	support	support	*	*
MANCHESTER	free	free	free	free	free	support	support	support
MII	support	support	support	support	support	support	support	support
PCI	support	*	*	*	*	*	*	*
PECI	support	support	support	support	support	support	support	support
PS/2	free	free	support	support	support	support	support	support
SD2.0/SDIO	support	support	support	support	support	support	*	*
UART(RS-232C/422/485)	free	free	free	free	free	free	free	free
USB1.1	free	support	support	support	support	support	support	support
1-WIRE	free	free	free	free	free	support	support	support
3-WIRE	support	support	support	support	support	support	support	support
I2C	free	free	free	free	free	free	free	free
I2C(EEPROM 24LX)	support	support	support	support	support	support	support	support
ISO7816 UART	support	support	support	support	support	support	support	support
SLE4442	support	support	support	support	support	support	support	support
SPI	free	free	free	free	free	free	free	free
SPI PLUS	support	support	support	support	support	support	support	support
UNI/O	support	support	support	support	support	support	support	support
AC97	support	support	support	support	support	support	support	support
HDA	support	support	support	support	support	support	*	*
IIS	free	free	support	support	support	support	support	support
PCM	support	support	support	support	support	support	support	support
S/PDIF	support	support	support	support	support	support	support	support
ST	support	support	support	support	support	support	support	support
JTAG2.0	support	support	support	support	support	support	support	support

* Not support : We suggest 4 times sample rate to capture DIGRF, HDA, LPC, LPC-SERIRQ and SD2.0/SDIO. MCU-51 DECODE needs 18 channels. PCI needs 47 channels.

Automotive PC System Memory Digital Audio IC Interface Basic Logic Application Other

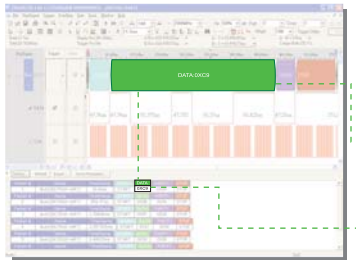
Protocol Analyzer

Product Model / Protocol Analyzer	LAP-B(702000+)	LAP-C(322000)	LAP-C(321000)	LAP-C(32128)	LAP-C(162000)	LAP-C(16128)	LAP-C(16064)	LAP-C(16032)
MCU-51 DECODE	support	support	support	support	*	*	*	*
MICROWIRE	free	free	free	free	free	support	support	support
SSI	free	free	free	free	free	support	support	support
ARITHMETIC LOGIC	support	support	support	support	support	support	support	support
DIGITAL LOGIC	support	support	support	support	support	support	support	support
JK FLIP-FLOP	support	support	support	support	support	support	support	support
UP DOWN COUNTER	support	support	support	support	support	support	support	support
7-SEGMENT LED	free	free	free	free	free	free	free	free
CCIR656	support	support	support	support	support	support	support	support
DALI	support	support	support	support	support	support	support	support
DIGRF	support	support	support	support	support	support	*	*
DMX512	support	support	support	support	support	support	support	support
DSA	support	support	support	support	support	support	support	support
HDQ	free	free	free	support	support	support	support	support
IRDA	support	support	support	support	support	support	support	support
LCD 12864	support	support	support	support	support	support	support	support
LCD 1602	support	support	support	support	support	support	support	support
MILLER	free	free	free	free	free	support	support	support
MOD	support	support	support	support	support	support	support	support
MODIFIED MILLER	support	support	support	support	support	support	support	support
MODIFIED SPI	support	support	support	support	support	support	support	support
NEC PD6122	support	support	support	support	support	support	support	support
PM1.1	support	support	support	support	support	support	support	support
PSB	support	support	support	support	support	support	support	support
SDQ	support	support	support	support	support	support	support	support
SIGNIA 6210	support	support	support	support	support	support	support	support
SM2.0	support	support	support	support	support	support	support	support
ST7669	support	support	support	support	support	support	support	support
WIEGAND	support	support	support	support	support	support	support	support

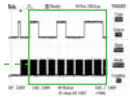
* Not support : We suggest 4 times sample rate to capture DIGRF, HDA, LPC, LPC-SERIRQ and SD2.0/SDIO. MCU-51 DECODE needs 18 channels. PCI needs 47 channels.

Application Field of Protocol Analyzer

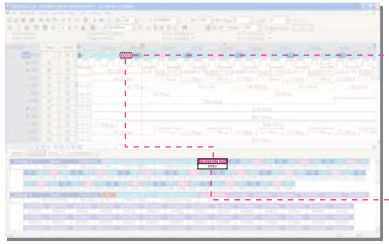
ISO7816 UART



```
ISO7816MainLoop:
        MOV   A,#16
        MOV   ETU,A
        MOV   A,#8
        MOV
ISOSEND,A
Loop1:
        BS    PTD,PTD0
        MOV   A,0XC9
        CALL  DelayNus
```



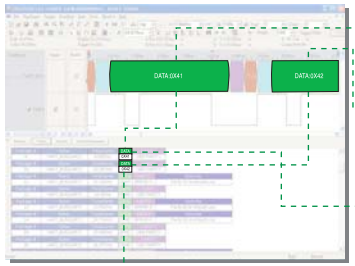
CCIR656



```
MAIN_CCIR656:
        CALL
INITIAL_CCIR656
        MOV   INTEGER,A
        MOV   DECIMAL,A
        MOV   A,#0X80
        MOV   SAV_EAV,A
        CALL
SAV_EAV_CCIR656
        CALL
OUTPUT_CCIR656
```

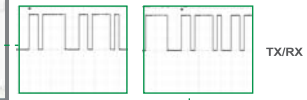
Oscilloscope can't be applied due to shortage of testing channels.

UART



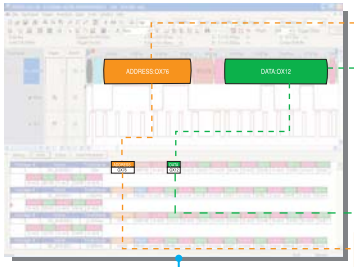
```
UART DataBitLoop:
MOV   A,#0x41 ; UART DATA SET = 0x41
MOV   UARTDatabit1, A
MOV   UARTDatabit2, A

UART DataByteLoop1:
MOV   A, #0x42 ; UART DATA SET = 0x42
XOR   A, UARTDatabit2
JBS   STATUS,  Z , UARTDataByteOff
```

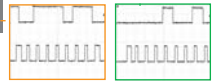


TX/RX

IIC



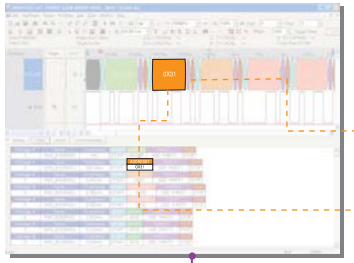
```
IIC AddressSet :
MOV   A,#0x76 ; IIC Address set 0X76
        MOV   Addressbit,A
        JMP
IIC DataSet :
MOV   A,#0x12 ; IIC Data Set 0X12
        MOV   Databit01,A
        MOV   Databit02,A
        JMP   IICDataInit2
```



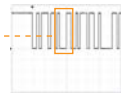
SDA

SCL

MOD

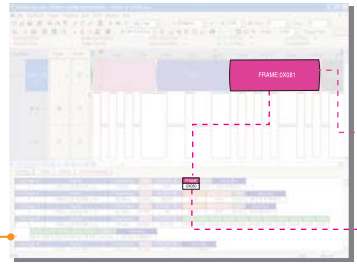


```
OUTPUT_ADDRESS_MOD_RTU_1 :
TBRDP MOD_DATA
CALL  OUTPUT_MOD_RTU
DJZ   TABLE_LENGTH_MOD,$+3
JMP   OUTPUT_TABLE_MOD_RTU_1
CALL  OUTPUT_CRC_RTU_1
CALL  DELAY1MS_MOD_IDLE
MOV   A, 0X31 ; ADDRESS = 0X31
MOV   TABLE_LENGTH_MOD, A
```



MOD

USB1.1

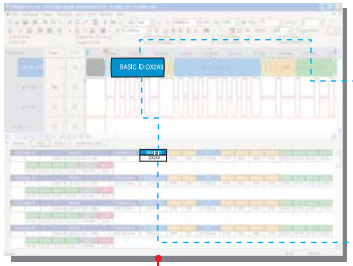


```
FRAME_START:
MOV   A,#0X02
MOV   PTD,A
CALL  DELAY4667NS
MOV   A, FRAME_LENGTH_TEMP
ADD   A, #0X01
MOV   TABLE_LENGTH_USB,A
MOV   A,0X080 ; Frame = 0x080
```

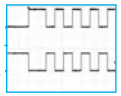
D+

D-

CAN 2.0B

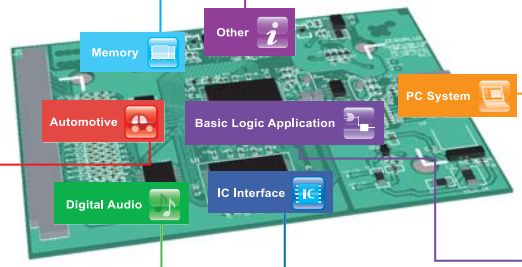


```
CAN 2.0B MainLoop :
Call  CAN_Init
Call  CAN_Start ;Start
mov   A,#0x55 ;
Basic_ID = 0X2A9(16) = 01010101011(2)
mov   CAN_ID, A
Call  CAN_ID_Loop
CAN_ID_Loop:
RLC   CAN_ID,#1
jbs   STATUS,C,CAN_IDBitHigh
jmp   CAN_IDBitLow
```

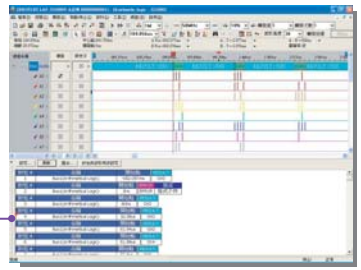


CAN_H

CAN_L



ARITHMETIC LOGIC



Half Adder

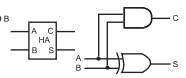
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

True Table

C=A · B

S=$\bar{A}$B+A$\bar{B}$=A ⊕ B

True Table



Ci	A	B	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Co=$\bar{C}$iAB+C$\bar{A}$B+CiA$\bar{B}$+CiAB

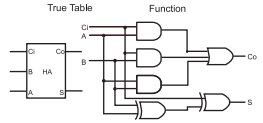
=CiA+CiB+AB

S=$\bar{C}$i$\bar{A}$B+$\bar{C}$iA$\bar{B}$+C$\bar{i}$A$\bar{B}$+CiAB

=Ci ⊕ A ⊕ B

True Table

Function



Half Subtract

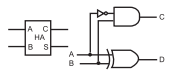
A	B	C	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

True Table

C=A · B

D=$\bar{A}$B+A$\bar{B}$=A ⊕ B

Function



Ci	A	B	Co	D
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Co=$\bar{C}$iAB+C$\bar{A}$B+CiA$\bar{B}$+CiAB

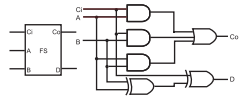
=$\bar{A}$B+C$\bar{A}$+CiB

S=$\bar{C}$i$\bar{A}$B+$\bar{C}$iA$\bar{B}$+C$\bar{i}$A$\bar{B}$+CiAB

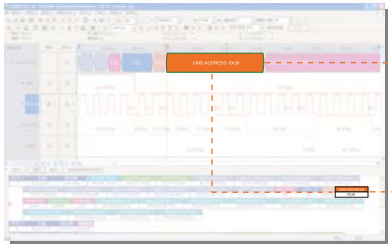
=Ci ⊕ A ⊕ B

True Table

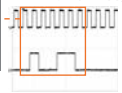
Function



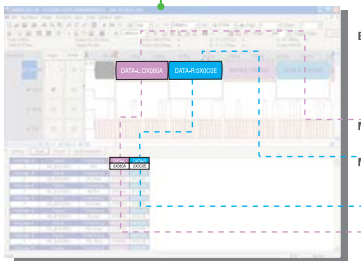
AC97



```
Initial:
        BC    SystemFlag,CheckKey
        BC    SystemFlag,SendFlag
        MOV   A,#0X26
        MOV   IOCA,A
        MOV   A,#0XFF
        MOV   IOCA,A
        MOV   PUCA,A
        MOV   IOCC,A
        MOV   PUCC,A
        MOV   PTF,A
        BC    STATUS,C
```



IIS

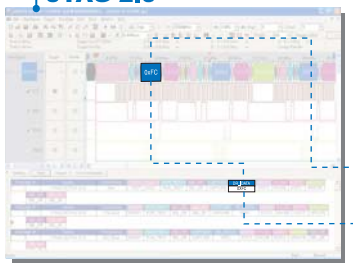


```
IIS Initial :
BC    SystemFlag,CheckKey
        BC SystemFlag,SendFlag
        BC PTF,PTF0
        BS PTD,PTD1
        CALL DELAY400NS
MOV A,#0X080A ; IIS DATA = 0X080A
        MOV COUNT2,A
MOV A,#0X0C0E ; IIS DATA = 0X0C0E
        MOV COUNT1,A
        BC PTD,PTD1
```

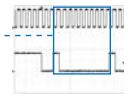
SDA

SCLK

JTAG 2.0



```
JTAG 2.0 Modelinitial:
BC    SystemFlag,CheckKey
MOV   A,#0x01
MOV   _gTMove0,A
CALL_JTAGINIT
CALL_JTAG_TAP_SLELogicReset
CALL_JTAG_SelectDRScan
CALL_JTAG_TAP_SLELogicReset
MOV A, 0x0FC ; Data = 0xFC
BS    PTF,PTF0
```



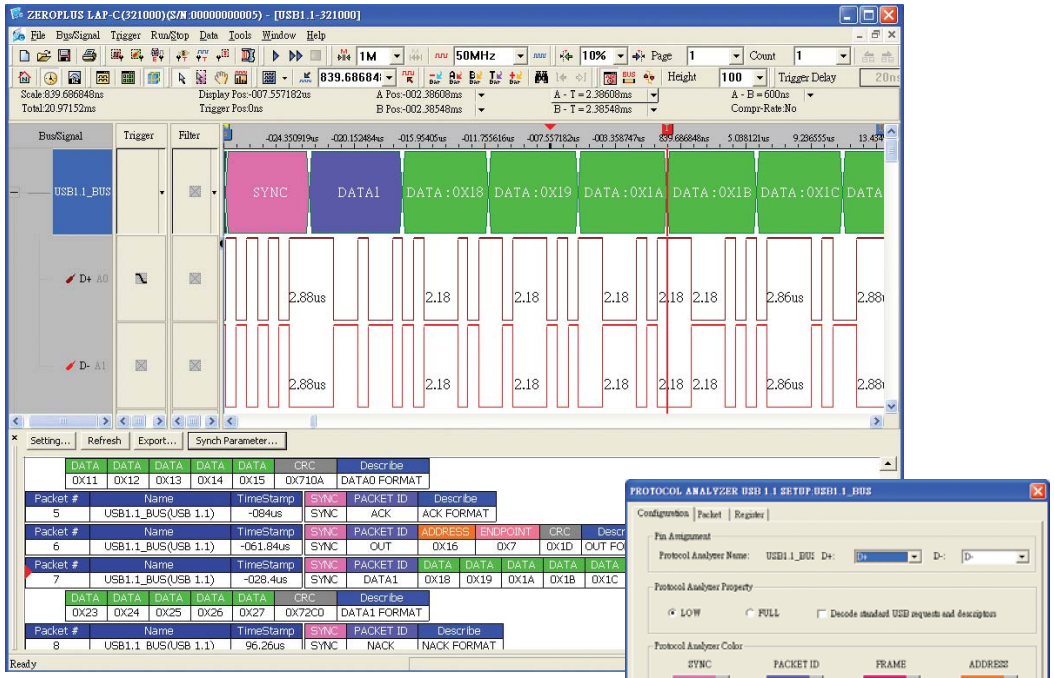
TCK

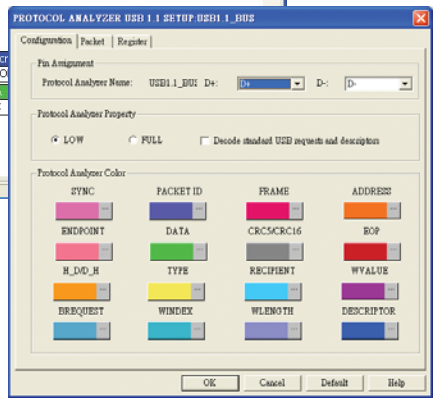
TMS

Application Field of Protocol Analyzer

USB1.1

ZEROPLUS Logic Analyzer can analyze the packets of the USB which is classified into Low Speed and Full Speed. The analytical result is as below. Only when users connect the D+, D- and GND line of the USB1.1 to the LA, and activate the function of analyzing the packet of the USB1.1, can the information of the USB1.1's packets be seen.





The below is the interface of the USB1.1. Users only need to set the D+ and D- of the USB1.1 and select the corresponding speed (USB1.1 or USB1.0), then they can analyze the status of the signal easily.

ZEROPLUS Protocol Analyzer Award

Free Get Three Protocols!!

ZEROPLUS hold the [Protocol Analyzer Award] to solicit more and more protocol analysis module. Welcome all the R&D engineers to take party in this activity. Users can download ZEROPLUS SDK (Software Development Kit) to develop more Protocol Decoding Modules and share them to public. ZEROPLUS will offer three protocol decoding module freely to the candidates who will have submitted good creations as an encouragement.

Website: http://www.zeroplus.com.tw/EDM/20090713/SDK_en.html

ZEROPLUS Logic Analyzer is widely used in the steps of hardware and firmware debugs for IC Design, Consumer Electronics, Automotive, Medical Electronics, Power Electronics, Avionics, Communication Network, Intelligent Building, Intelligent Traffic and different kinds of the Industrial Automation, etc..

Automotive
CAN 2.0B / FLEXRAY 2.1A / LIN 2.1

Memory
1-WIRE / 3-WIRE / I2C / I2C(EEPROM 24LX) / ISO7816 UART / SLE4442 / SPI / SPI PLUS / UNI/O

Digital Audio
AC97 / IIS / PCM / S/PDIF / ST

LAP-C Series

LAP-B Series

PC System
LPC / LPC-SERIRQ / MANCHESTER / MII / PCI / PECI / PS/2 / SD2.0/SDIO / UART(RS-232C/422/485) / USB 1.1

IC Interface
JTAG 2.0 / MCU-51 DECODE / MICROWIRE / SSI

Basic Logic Application
ARITHMETIC LOGIC
DIGITAL LOGIC
JK FLIP-FLOP
UP DOWN COUNTER

Other
7-SEGMENT LED / CCIR656 / DALI / DIGRF / DMX512 / DSA / HDQ / IRDA / LCD1602 / LCD 12864 / MILLER / MOD / MODIFIED MILLER / MODIFIED SPI / NEC PD6122 / PM 1.1 / PSB / SDQ / SIGNIA 6210 / SM2.0 / ST7669 / WIEGAND

Our Customers

Manufacturers of China

- SHENZHEN HANGSHENG ELECTRONICS CO., LTD.
- SINOWEALTH Electronic (Shanghai) Ltd.
- Fulhua Microelectronics Corp.
- CLX Technology Co., Ltd.
- Arkmicro Technologies Inc.
- Shenzhen LOKEE Technology Development Co., Ltd.
- Shenzhen CO-TRUST technology Co.,Ltd.
- HYT Science & Technology Co., Ltd.
- Foxconn Technology Group
- Shenzhen Jiuzhou Optoelectronics Co., Ltd
- Fujian Polytechnic of Information Technology

Consumer Electronics

- Quanta Computer, Inc.
- MSI Computer Corp.
- Sunplus Technology Co., Ltd.
- Inventec Corp.
- ASUSTek Computer, Inc.
- Mitac International Corp.
- Yamaha KHS Music Co., Ltd.
- Transcend Informational, Inc.
- Qisda Corp.
- Logitech, Inc.
- Cheng Uei Precision Industry Co., Ltd.
- TECOM Co., Ltd.

IC Design

- ATMEL Corp.
- Winbond Electronics Corp.
- SiliconMotion Technology Corp.
- ELAN Microelectronics Corp.
- RENESAS Technology Corp.
- Realtek Semiconductor Corp.
- Sonix Technology Co.,Ltd.
- Novatek Microelectronics Corp.
- Broadcom Corporation
- Mstar Semiconductor, Inc.

Academic Research

- National Taipei University of Technology
- ACADEMIA SINICA
- National Chiao Tung University
- LUNGHWA University of Science and Technology
- National Taiwan University
- Southern Taiwan University
- Industrial Technology Research Institute
- Tamkang University
- National Tsing Hua University
- National Cheng Kung University

Automotive

- Automotive Research & Testing Center
- Hua-chuang Automobile Information Technical Center Co., Ltd.

Optical Electronics

- EVE LIGHT Technology
- Silicon Optronics, Inc
- Top Powersonic Co., Ltd.

Industrial Computer

- Unitech Electronics Co,. Ltd.

Other

- Secom Co., Ltd.

Industrial Control

- TECO Electric & Machinery Co., Ltd.
- Far Eastern Textile Co., Ltd.

Our Customers

YAMAHA KHS Music Co., Ltd
YAMAHA Semiconductor Technological Center
Director of the RD Division
Mr. Lin Hai-li

"ZEROPLUS Logic Analyzer is my secret weapon."

The businesses of the YAMAHA group are extremely comprehensive, including in areas of life, culture and leisure. The new goal for the business aims to have "sound" and "music" as the central structure of the group. Every undertaking should be dedicated to enhance the competitiveness of the business. Through the close link and cooperation with other sectors, the group can perform with superiority.

Regarding the procurement of ZEROPLUS Logic Analyzer, Mr. Lin Hai-li, the director of the YAMAHA RD District said, When we started to research online for an appropriate Logic Analyzer, only few met our requirements. Without much expectation, we contacted Ms. Lin Gia-fang in ZEROPLUS and were impressed by her professional introduction, which gave me confidence in Zeroplus products. Unlike big logic analyzers, ZEROPLUS PC-Based Logic Analyzer is equipped with standard features. Compact as it is, this Logic Analyzer has everything.

After procurement, Ms. Lin in ZEROPLUS kept updating the software and product information. She took a very proactive role in the after-sale service. Where there were small problems with the machine, she would talk to the engineers to get rid of the problems. The extra features of I2C, UART, SPI serial signal decoding of ZEROPLUS Logic Analyzer made the price worthy.

When I was using ZEROPLUS Logic Analyzer at the client end, many engineers fancy that they can have one. The problem of software/hardware debug happens to both software and hardware engineers. When the problem is directed to the software, the software engineers believed the cause was from the hardware. Therefore, the Logic Analyzer was served as an arbitrator. Take I2C control for example, the software engineers believed the problem came from the wrong wiring whereas the hardware engineers reckoned the problem was from the wrong ID sent by the software. To resolve the dispute, one can connect the Logic Analyzer to record the hardware control process and everything can become really clear.

Both hardware and software engineers believe that if one compact Logic Analyzer can be placed on the table, the trouble of borrowing a big one can be saved and staffs would no longer fight fault with each other. This Logic Analyzer indeed saves me a lot of time debugging. With only a few minutes, I can locate the problems that have been bothering clients for days. Logic Analyzer is a great debug tool with superior design. I think smart engineers would make use of the best debug tools to facilitate their work. ZEROPLUS Logic Analyzer is my best secret weapon.

ASUSTek Computer Inc.
CM5, Broadband RD Division
RD engineer
Mr. Lin Kuo-Yang

"The sooner is the debug, the shorter the RD of products takes."

ASUSTek Computer Inc. (or ASUS) is a leader in the 3C total solutions in the consumer electronic industry. With a complete product portfolio, the company helps users in every field create the optimal performance. ASUS products are comprehensive, including the standard desktop systems, servers, notebooks, LCD monitors, LCD TVs, cabinets/power supply/coolers, handheld PCs, broadband network equipment, wireless communications equipment, digital information house appliances, and mobile phones.

Mr. Lin Kuo-yang from CM5 of the Broadband RD Division, where the focus is on Set-up Box, ADSL Modem and Cable Modem, is responsible for the design of embedded system, other systems and software.

Mr. Lin shared his work experience of the current stage: with regard to the measure of the Karaoke processing chip of the YAMAHA YS-915 sound card, obstacles appeared during the development of its drivers. Uncertainty about whether signals on the SPI interface can be correctly transmitted was there so we adopted ZEROPLUS LAP-A(32128) PC-Based Logic Analyzer and the signal transmission was then stable. To check whether the logic between the circuit and the program is correct during the RD phase can rapidly identify and get rid of the problem on the hardware or the software. Mr. Lin in great joy said, "The sooner is the debug, the shorter the RD of products takes."

As pointed out by Mr. Lin Kuo-yang from Asus, ZEROPLUS Logic Analyzer is compact and light, unlike the bulkiness of those traditional machines. This transformation facilitates the construction in a measure environment and creates neatness. The patented compression feature of ZEROPLUS Logic Analyzer can lengthen the measure depth and capture more signals for one analysis. Compared with the depth provided by traditional machines, ZEROPLUS Logic Analyzer is much more economic. In addition, the user-friendly interface allows beginners to start operating the machine right away and serves as a spring board for users of traditional machines as well as a good teaching method. What comes to attention is that the feature of direct analysis of the LAP-A special BUS is very practical. When the measure objects are such common Buses as SPI and UART, the complicate calculation of 0010 is not necessary, which is a great tool for developing dirvers.

ZEROPLUS Logic Analyzer: Redefine the R&D possibilities, Reduce the time and cost. Possess excellent design edges. With it, you can make everything possible.

Accessory

Testing cable (25 cm)

package of 16 channel model
Including:
25 cm, 8 pin testing cables*2
25 cm, 2 pin testing cables*1
25 cm, 1 pin testing cable*1

Testing cable (40 cm)

package of 16 channel model
Including:
40 cm, 8 pin testing cables*2
40 cm, 2 pin testing cables*1
40 cm, 1 pin testing cable*1

Testing cable (25 cm)

package of 32 channel model
25 cm, 16 pin testing cables*1
25 cm, 8 pin testing cables*2
25 cm, 2 pin testing cables*1
25 cm, 1 pin testing cable*1

Testing cable (40 cm)

package of 32 channel model
40 cm, 16 pin testing cables*1
40 cm, 8 pin testing cables*2
40 cm, 2 pin testing cables*1
40 cm, 1 pin testing cable*1

Logic analyzer Carry Bag

200(L)*150(W)*45(H)mm

package of LAP-C Series

Probe (test hooks)

20 pieces/package

Probe (test hooks)

36 pieces/package

USB Cable 1.5M

AC Power Cable

package of LAP-B series

BNC Cable

package of LAP-B series

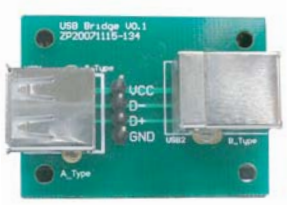
Pulse Width Trigger Module

- Pulse Width Trigger Module *1
- Test Cable (7pins)*1
- Test Cable (2pins)*1
- User Guide *1

5.4cm(L) * 4.5cm(W) * 1.8cm(H) 50g

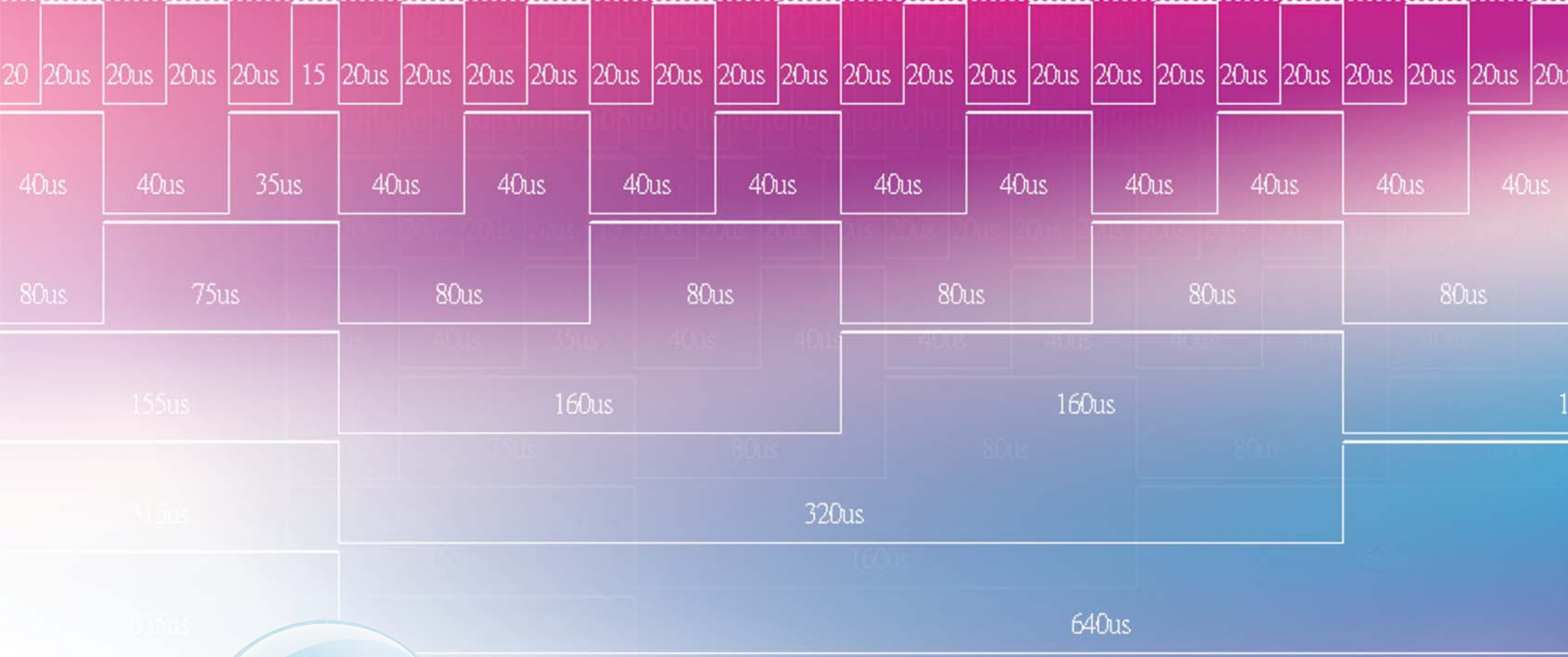
USB Bridge

Including:
USB Bridge
USB Cable



DIP IC Test Clips

8 Pins, 14 Pins, 16 Pins, 18 Pins, 20 Pins, 22 Pins, 24 Pins, 28 Pins, 36 Pins, 40 Pins, 48 Pins, 64 Pins



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